Riviera-PRO 2012.06

Release Notes

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Release Notes for Riviera-PRO 2012.06

What's New

Performance Improvements

- Compilation of projects based on UVM libraries runs up to 30% faster in comparison with previous Riviera-PRO versions. (SPT63918)

SystemVerilog Simulation

- Subarrays of unpacked fixed-size arrays can be used in blocking assignments. (SPT62546)
- It is possible to use empty assignment patterns ('{}) and unpacked array concatenations ({}) as default values for task and function arguments of the dynamic array and associative array type. (SPT63585)
- The conditional if-else statement can now be used in the context of the random constraint blocks. (SPT48276, SPT63728, SPT49750)
- The size() method for queues and dynamic arrays can be used in the constraint blocks. In the current version, the functionality is limited to the constraint blocks declared in classes. The method cannot be used in the inline constraints and with the std::randomize() function. (SPT48954, SPT51143, SPT60649, SPT62525, SPT62619, SPT63299)
- The dynamic casting to enumerated types is supported. (SPT63915)

```
module top;
  enum bit [1:0]{RED = 2'b00, BLUE = 2'b01, WHITE = 2'b10} col_e;
  bit [1:0] col_b = 2'b01;

  initial
    $cast(col_e, col_b);
endmodule
```

- Extern declarations of program blocks are supported.
- Constants of the string type declared as a user-defined forwarded type are supported. For example:

```
typedef T_string;
const T_string str1="test_string";
// ...
typedef string T_string;
```

- Specparams can be declared as vectors.

```
specparam [3:0] y  = 4'b0101;
```

OVM and UVM Libraries

- Riviera-PRO introduces support for the VMM 1.1.1a library. This library is not delivered with the installation of Riviera-PRO. To obtain the VMM library compatible with the current release of Riviera-PRO, contact Aldec Support. (SPT60272)
- The UVM library version 1.1b is now supported and is considered as the default library version. The precompiled UVM 1.1b library (uvm_1_1b) is delivered with Riviera-PRO and mapped as uvm. The previous version 1.1a has been removed.
- The UVM library has been enhanced with the new argument +UVM_SET_ALDEC_DEFAULT_RECORDER that allows setting the Aldec recorder as the default one that will be used in the cases when the recorder is not specified explicitly. The Aldec recorder (UVM_RECORDER_ALDEC) is an Aldec's implementation of the UVM_RECORDER class that extends its functionality allowing transactions to be recorded in the ASDB simulation database. The use of already existing UVM arguments has been also changed. Now, to set the ALDEC recorder for all components in the project, the UVM arguments +UVM_ALDEC_RECORDING +UVM_SET_RECORDING_DETAIL have to be specified in the asim command instead of the +UVM_ALDEC_RECORDING=ALL argument that enabled this setting in previous versions.
- The UVM libraries are supplemented with the precompiled version of the DPI library for regular expression matching.

DPI Interface

- The SLP acceleration is now available for functions imported from the C side of the DPI interface.

Mixed VHDL and SystemVerilog Simulation

- SystemVerilog parameters of the array type can be used as generics of VHDL entities instantiated as SystemVerilog modules. For example:

  VHDL:

```
library ieee;
use ieee.std_logic_1164.all;

package my_types is
  type type_array is array (0 to 3) of std_logic_vector(3 downto 0);
end;

use work.my_types.all;
entity top is
  generic ( g1 : type_array:=(others=>(others=>'0')) );
end;

architecture arch of top is
begin
end;
```

  SystemVerilog:

```
module tb;
  typedef logic [3:0] type_array [0:3];
```

```
  parameter type_array a1= '{1,2,3,4};

  top #(.g1(a1))t1();
endmodule
```

(SPT50901)

VCD Files

- SystemVerilog packed structures and packed unions can be dumped to VCD files.

Interface to SystemVue

- The SystemVue interface that allows performing a co-simulation with the Agilent SystemVue® software is now available. Agilent SystemVue is an electronic design automation environment for electronic system-level designs that is particularly dedicated to RF, DSP, and FPGA/ASIC implementers.

  After a successful compilation, the SystemVue export files can be created either by using the new systemvuegenmod command or by right-clicking a library item in the Library Manager window and selecting the Generate Library for SystemVue option. The files can be further imported to the SystemVue tool to set up a co-simulation environment with Rivera-PRO working as a server that simulates the HDL blocks in the SystemVue schematic design. (SPT63601)

Macro Commands

- The acdb include and acdb exclude commands have been implemented. The new commands allow including or excluding from statistics stored in an ACDB database selected types of coverage data that will be then presented in a coverage report. For example, the acdb exclude command allows omitting in the report statistics for user-defined design regions, instances, or information about execution of statements in specified lines of source code. (SPT61935)
- The acdb report command has been enhanced and supplemented with new arguments which allow filtering coverage statistics included in the report per design unit or per instance name. For more information, refer to the description of the acdb report command.
- The -allow_duplicated_units argument for the alog command has an impact on primitive declarations. In previous versions, the -allow_duplicated_units argument affected unit declarations only. (SPT63211)
- The -glitch argument has been added to the syntax of the asdbcompare command. The new argument allows comparing waveforms with delta accuracy.
- The -value_matching argument for asdbcompare command has been added. The new argument specifies which signal values will be considered identical in the comparison process.
- The -immediate argument has been added to the syntax of the cover report command. When the new argument is passed, a report with coverage data is supplemented with statistics for expressions of immediate cover.
- VHDL arrays that have ranges of an enumerated type can now have the ranges designated by enumeration values when specifying the object name for the examine command. (SPT62395)
- The mem load command is available. The command allows loading data from standard Verilog hex and binary memory pattern file formats to unpacked arrays of packed data. (SPT60322, SPT60451, SPT60849)

- The precision command has been introduced. The command allows specifying the number of digits to be displayed after the decimal point.
- The simulation.object.event.next and simulation.object.event.prev commands are introduced. The commands display on the console a string with the time of the nearest next or previous event that occurred on the object specified with the object parameter. If there is no next or previous events, the command returns empty string.

  ```
  simulation.object.event.next [-delta] [-time <time>] <object>
  simulation.object.event.prev [-delta] [-time <time>] <object>
  ```

  The optional -time argument specifies the beginning time from which the event will be searched. If not specified, the current simulation time is used. The optional -delta argument specifies whether the delta is to be included in the resulting string. By default, deltas are skipped.
- The wave command has been enhanced with new arguments: -expand and -child that allow displaying elements of aggregates in the Waveform Viewer. The -expand argument can be applied to vectors, arrays, records, virtual objects, etc. and specifies that the aggregate added to the waveform is to be expanded. The -child argument is used to specify properties of aggregate elements. The properties, such as: value format, shape (literal or analog), color and height of the waveform can be set for each element of an aggregate by placing the appropriate arguments and the object name after the -child argument, for example:

  ```
  add wave -expand /tb/UUT/data_in ( -child ( -expand -height 50
  -analog /tb/UUT/data_in.r ) )
  ```

  (SPT63037)

Framework

- The Enable tooltips option has been added to the Tools | Customize | Options category of the Customize dialog box. It turns on/off the display of tooltips in Riviera-PRO. (SPT63073)

Waveform Viewer

- Object property settings (such as radix, height, shape and so on) are recorded to .awc file for signals which are vector or array elements, record fields, or members of virtual objects. The information whether these aggregates were expanded or collapsed is also collected. (SPT61998, SPT63111)
- The display of values of the enumerated and string types has been improved. If the whole string or the enumerated type object (either VHDL or Verilog) cannot be displayed in the Waveform View pane, it is truncated on the right-hand side (if the values are left-aligned in the Waveform View pane). Similarly, if the values are right-aligned, it is truncated on the left-hand side or truncated on both sides if the values are centered. The truncated values are marked with ellipsis (...). For example, open_gate is truncated to op... . (SPT63789)
- The way in which cursors are displayed has been improved in order to facilitate the work with the Waveform Viewer in cases when a greater number of cursors or subcursors are in use. When a subcursor prevents the active cursor from being moved to the left, for example when a subcursor reaches 0ps and cannot move further, the subcursor will start blinking to let the user know which subcursor is blocking the active cursor. If a subcursor is collapsed, the parent cursor will blink instead. If there are several nesting levels and all are collapsed, the rule is that the outermost parent cursor will blink. (SPT63225)

- The Show Frequency in Measurement option was removed from the Tools | Waveform Viewer | Display category of the Preferences dialog box. Instead, the Set All Measurement Units option has been added to the context menu in the Cursor View pane. It allows setting time or frequency measurement unit for all cursors in the active waveform window. Additionally, the Toggle Measurement Unit option has been replaced with the Set Measurement Unit option which allows setting time or frequency measurement unit for the active cursor. (SPT63580)

Hierarchy Viewer

- The Show Hierarchy Find Results button for showing search results of the Hierarchy Find was added. The button is available on the main toolbar.

HDL Editor

- The Show in Outline option has been added to the context menu of the HDL Editor. When the Outline window is closed, the option opens the window and shows the object selected in the HDL Editor.
- The code templates for UVM have been added. The templates are available in macros and SystemVerilog source code.
- The custom code templates can now be created from the selected code in the HDL Editor by using the Block | Create Template option from the context menu.
- The Create Variable option has been added to Code Templates. To create a new variable, select the text in Template editor and choose the Create Variable option from the context menu.
- Tooltips with declaration of identifiers in VHDL code are available when source code analysis is enabled. Note that the simulation does not have to be initialized to view those tooltips.
- The usability of the template auto-complete mechanism has been improved - it is faster and more intuitive. Pressing the Enter key will move the insertion point to the first location of the ${cursor} instead of inserting a new line. Pressing the Escape key will leave the template and the insertion point in the currently edited location.

Outline Window

- Synchronization between the Outline window and the HDL Editor has been implemented. When this feature is enabled, inserting the mouse cursor in a line of an object declaration displays this object in bold in the Outline window.

Advanced Dataflow

- Hierarchical references are presented in Verilog designs. It is another way of showing signals passing through design hierarchies. It is visible if the signal comes from one hierarchy to another.
- The contents of the Advanced Dataflow window can be printed. It is also possible to display the items to be printed in the print preview. The Print and Print Preview options are available in the File menu. (SPT45817)

Message Viewer

- The functionality of the viewer has been enhanced. Messages displayed in the Messages window

can be filtered by the message type or the message text. Additionally, the progress bar is displayed at the bottom of the window while filtering or sorting items visible in the window.

Tasks Window

- The Tasks window has been implemented. It displays tasks scheduled to do in a project. The tasks can come from code analysis or can be defined by the user in the Tasks window. By default, Riviera-PRO recognizes tasks with the predefined tags: TODO and FIXME and has the possibility to create additional tags. The tags can be specified in the Tools | Tasks | Tags category of the Preferences dialog box.

Memory Viewer

- Support for Hexadecimal Verilog Memory Dump files (*.txt, *.hvmi) and for Binary Verilog Memory Dump files (*.txt, *.bvmi) has been added. Saving is not supported yet.

Design Manager

- The design manager window has been enhanced. The compilation options can now be specified for each source file in the workspace separately. The options can be accessed by right-clicking a file and selecting the Properties option. The compilation options specified here work for the selected file and override the design properties that can be set in the Compilation category of the design Properties dialog box. (SPT62004, SPT62408)

GUI Preferences

- The number of SystemVerilog compilation modes that can be selected using the Preferences dialog box has been extended. It is now possible to choose the LRM 1364-2005 mode from the drop-down list accessible in the Compilation | SystemVerilog | General category. The LRM 1364-2005 mode corresponds to the -v2k5 argument of the alog command.
- The Disable generation of vacuous reports for IF statements option has been added to the Compilation | VHDL | Assertions and Compilation | SystemVerilog | Assertions categories. The new option is equivalent of the -xevd argument of the acom or alog commands and it disables extended vacuous evaluation for the operators if and implies in SystemVerilog and for the operator -> in PSL.
- Logging of messages generated by the simulator can be controlled not only by using the command line but also by using the GUI settings. The Log simulation messages option available in the Simulation | Dataset category of the Preferences and design Properties dialog box allows selecting 4 types of messages: Assertions, Errors, Notes and Warnings to be logged to the database. Equivalent to the -logmsg parameter of the asim command.
- New options for assertions available in the Preferences | Simulation | Assertions | Assertion category, in the section related to failures, were added: Distinguish vacuous and nonvacuous failures, Track assertion nonvacuous failures, Track assertion vacuous failures and Track assertion extra failures. In the section related to passes the following options were added: Track assertion nonvacuous passes, Track assertion vacuous passes and Track assertion extra failures. In the section related to covers available in the Preferences | Simulation | Assertions | Cover category, the following options were added: Track cover nonvacuous matches, Track cover vacuous matches and Track cover extra matches.

Documentation

- The array manipulation methods have been described in the SystemVerilog Reference Guide. The description can be found in the section Arrays and Queues | Array Manipulation Methods. (SPT62867)

Miscellaneous

- The elements of VHDL arrays that are indexed by enumerated types can be accessed in the Riviera-PRO GUI using enumeration names. In previous versions, elements of such arrays could be accessed only by integer values of an enumerated type. (SPT48929, SPT62395)
- The Preview field of the Appearance category has been improved.
- The values in the Address column are displayed in bold for objects with address matched with the currently selected value in used debug windows (Object Viewer, Locals and Watch window).

Problems Corrected in Version 2012.06

Framework

- Now both File | Recent Directory and File | Change Directory menu options execute the cd command explicitly. (SPT63427)

VHDL Simulation

- An issue that terminated the simulation with an incorrect compilation error message for some particularly complex expressions containing arrays, record and function calls is now resolved. (SPT63448)
- A number of issues that appeared when determining the constant range with an attribute of value returned by a function are now fixed. (SPT63644, SPT63649)
- The following defects resulting in occurrence of compiler or simulator errors were fixed: SPT63308, SPT63907.

Verilog and SystemVerilog Simulation

- The simulator sometimes did not propagate values assigned to initialization through inout ports of the logic type. (SPT50776, SPT50788)
- Riviera-PRO could sometimes yield wrong simulation results for projects containing module instances with a part of their ports left unconnected. The problem revealed itself only in cases when the module declaration and module instances were located in different source files and the files were compiled in separate invocations of the alog command. In the current release, the problem is resolved. (SPT63857)
- A defect that under certain circumstances could terminate simulation of an UVM based project if project files were compiled in the separate compilation was fixed. (SPT63818)
- Referring to signals from Vital components via an external name could sometimes cause an elaboration error. (SPT61033)

- A problem that occasionally appeared on the Linux version when calling the connect_phase and run_phase UVM routines is fixed. (SPT61483)
- An issue of races between processes from different instances of a module sensitive to the same signal was fixed. The issue was specific for the SLP acceleration mode only. (SPT63095)
- An issue that could cause an unexpected termination of the simulation if a value returned by a function was used as a replication multiplier was fixed. The issue was specific for the SLP mode only. (SPT63352)
- A defect that occurred only in the SLP simulation mode resulting in an unexpected termination of the simulation when calling a task declared in the interface via virtual interface instance was fixed. (SPT63378)
- An issue that could lead to wrong simulation results when one of the bitwise binary operator operands was an unbased unsized literal and the latter was an expression that size was determined by the context is fixed. The issue was specific for the SLP acceleration mode only. (SPT63940)
- Placing multidimensional arrays of nets on a unit port list could sometimes yield incorrect simulation results. (SPT63119)
- Several defects related to the use of the -incr argument of the alog command that, under specific conditions, disturbed the compilation process, are now resolved. The -incr argument enables a mechanism that omits unchanged modules in subsequent compilation runs to improve the overall compiler performance. (SPT63161, SPT63274)
- An issue that resulted in an unexpected termination of the simulation for projects containing virtual interfaces was fixed. The issue appeared only for the projects compiled with the -incr argument for the alog command. (SPT63250)
- Under some circumstances, Riviera-PRO could terminate simulation unexpectedly or yield incorrect simulation results when an argument of an unpacked array type was passed by value to a class method. This issue is now resolved. (SPT63260, SPT63318)
- The issue of a simulation termination that could occur when a class method was called from a method of another class if the method call was placed in a nested fork-join block is resolved. The resolved issue occurred only in cases when the called method was a member of array of classes. (SPT63880)
- An issue that resulted in an unexpected simulation termination which might appear when the string methods such as: atoi(), atohex(), atobin() etc. were used for an element of a queue, dynamic or associative array is resolved. (SPT63176)
- A problem that could cause wrong simulation results when values returned by the string methods, such as atoi or atohex, were added to a queue was fixed. The problem appeared when the string methods were called from an automatic function and took automatic variables of the string type as parameters. (SPT63221)
- An issue that could cause an unexpected simulation termination of designs containing a function that instead of explicitly defined type returned by that function had the unsigned keyword in its header was resolved. (SPT64132)
- The compilation could be unexpectedly terminated in cases that the streaming unpack operator (>>) was applied to the concatenation of packed structures. The problem occurred only if the operator was used inside a function and the slice_size was specified implicitly (e.g. as a data type). In the current version, the problem is resolved. (SPT64073)
- An issue that occurred when a queue, associative, or dynamic array was a type of a module port with a connection type specified as ref is now resolved. (SPT63227)

- A defect that in some situations caused the latter of two subsequent compiler runs to fail is now fixed. The problem appeared only during source files recompilation. (SPT63270)
- The simulation could sometimes terminate with an error message when the wildcard syntax (.*) was applied to specify interface port connections. This problem appeared only for the interfaces declared under the generate construct and in the current version is resolved. (SPT63355)
- An issue resulting in a performance loss and an excessive memory allocation when calling a class method recursively was fixed. The issue appeared when the method called recursively took a method returning an object as a parameter. (SPT63620)

```
class class_A;
  int data [1024];

  function class_A func_2();
    return null;
  endfunction : func_2

  function void func_1(class_A t);
    func_1(func_2());
  endfunction

endclass : class_A
```

- Several defects related to using empty array literals ({}) and pattern assignments ('{}) on the task or function port were fixed. An empty pattern assignment passed to a routine as a parameter now does not cause simulation problems. The problem with empty array literals and pattern assignments used as a default task or function task parameter is resolved too. (SPT63595)
- An issue that under some circumstances resulted in erroneous simulator behavior during randomization of aggregate types that were members of a virtual class is now fixed. The issue might appear when randomizing queues, associative arrays, or dynamic arrays if the array element was an instance of the class in which the rand statement was used. (SPT63597)
- An issue of the super keyword used in the expression that specifies whether the if or else part of the if...else condition is to be evaluated was resolved. In the current release, the super keyword can be used in this context. (SPT63586)
- An issue of the misleading error message: Call to undefined Verilog far function that could appear during simulation of UVM-based projects was resolved. (SPT63501)
- An issue that could appear when a recursive call to a method was placed inside a string concatenation is now fixed. (SPT63392)
- An issue, resulting in reporting an incorrect error message about a missing modport declaration that might sometimes occur when specifying the module port type as an unpacked array of modports is now fixed. (SPT63369)
- A problem resulting in an endless simulation run that could sometimes appear if the disable statement was applied to a fork-join block placed in a task which was a class method is now resolved. The problem appeared when a task was called from another method which was terminated with the kill() function from the built-in process class. (SPT63374)
- The following defects resulting in occurrence of compiler or simulator errors were fixed: SPT63393, SPT63498, SPT63518, SPT63689, SPT63897, SPT63902, SPT64003.

SystemVerilog/PSL Assertions

- A problem that occurred if the nonoverlapped implication operator (|=>) was used in the context of a multiclock property when one of the clocks was used in another property or sequence is now resolved. (SPT49002)

DPI

- Passing open arrays to the DPI function could terminate simulation if the import statement was placed in the compilation unit scope or inside a package. Now this issue is resolved. (SPT62813)
- In previous versions, Riviera-PRO did not display any meaningful message when a DPI C function to which an open array was passed had a wrong parameter type. In the current version, when the parameter type does not correspond to the open array element type, a warning message is displayed. (SPT61409)
- An issue that caused properties of dynamic arrays passed to the C side of the DPI interface were read incorrectly is now fixed. (SPT62812)
- Passing arrays of the unsigned byte type to DPI functions does not produce incorrect results in the current release. (SPT62811)

Mixed VHDL and SystemVerilog Simulation

- The issue of signals propagated from a SystemVerilog instance to a series of VHDL units and then back to a SystemVerilog instance that could be sometimes improperly evaluated is now resolved. (SPT63051)
- In some situations, the conv_std_logic_vector VHDL function from the package std_logic_arith package could cause an unexpected termination of the simulation process. The issue was resolved. (SPT63171)
- The following defects resulting in occurrence of compiler or simulator errors were fixed: SPT63639, SPT63884.

Mixed VHDL and SystemC Simulation

- A malfunction that resulted in a noticeable drop of the simulation performance when using the -logmsg all argument for the asim command is now fixed. The problem appeared only for the mixed VHDL and SystemC simulation. (SPT63563)

Toggle Coverage

- Previously, in some situations Toggle Coverage could affect displaying simulation data in the Waveform Viewer, which in turn could result in an unexpected application error. This issue was resolved. (SPT63314)

Macro Commands

- A problem with specifying a library location if the path designated by the VSIMSALIBRARYCFG variable stored a string representing a relative path containing /./ is now resolved. (SPT61922)
- A defect that made setting breakpoints impossible if the path to the files to be compiled was

specified with a symbolic link was fixed. (SPT63269)

Library Manager

- An issue with the Library Manager that did not refresh the library contents properly was fixed. (SPT63367)

Waveform Viewer

- Variables from the ieee_proposed.fixed_pkg package could be sometimes improperly displayed in the Waveform Viewer. This issue is now resolved. (SPT61646)
- Signal was improperly displayed in the Grid Settings dialog box if it was a member of virtual group. This issue was resolved. (SPT63959)

HDL Editor

- A malfunction that could sometimes cause Riviera-PRO to close unexpectedly when the source code analysis functionality was in use is now fixed. The issue appeared only on the Windows version of Riviera-PRO if the source files opened in the HDL Editor had the attribute set to read-only. (SPT63306, SPT63870)

Advanced Dataflow

- Previously, adding items to the Advanced Dataflow window in designs with many generate statements was slow. The issue was resolved. (SPT63473)

Interface to MATLAB

- The problem that could occur during a multiple use of the get_item and put_item functions to read/write elements of MATLAB arrays was resolved. The problem occurred only in cases when the get_item and put_item functions were called a great number of times and revealed itself with displaying the error message: Invalid object handle: <ADDRESS_VALUE> and reading wrong values from arrays. (SPT64025)

Miscellaneous

- The color of items selected and highlighted by the cursor has been changed. (SPT63469)
- An issue related to the VCD file format concerning redundant slashes at the beginning of variable names was resolved. The issue was only related to the vector variables and appeared when a VCD file generated in Riviera-PRO was opened in tools manufactured by other vendors. (SPT47465)
- A problem specific for older versions of the Qt library resulting in the error message:

  Application asked to unregister timer <NUMBER> which is not registered in this thread.

  has been resolved after upgrading the library to version 4.7.4. (SPT63235)
- An issue that under some circumstances could decrease the simulator performance under the Linux operating systems was resolved. The issue appeared when casting a vector variable to a string or when the substr(), toupper(), tolower() built-in methods were called. (SPT63366)

- Problem with truncating values in value tooltip was resolved. The ellipsis has been added to the end of the value which cannot fit into the tooltip. It appears on the right-hand side where the value is truncated. (SPT62436)

Reaching Technical Support

To open a Technical Support Case, users with a valid Maintenance Agreement should visit http://www.aldec.com/support. Please note, you will be asked to register if you have not already.

Diagnosing the problem may require information on the system where Riviera-PRO is running.

- Under Linux, this information can be collected with the system_info script delivered with Riviera-PRO. When running the script, specify the Riviera-PRO installation directory as the first argument.
- Under Windows, use the MSINFO32.EXE program.

NOTES

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