



## Main Product (LNTPRO)

Installed by main installation program

Feature	Additional License Part
<b>FRAMEWORK</b>	
GUI, Interactive Console and Batch modes	
Macro, Tcl, Perl script support	
<b>SUPPORTED STANDARDS</b>	
Verilog® IEEE 1364 (1995, and 2001)	
SystemVerilog® IEEE 1800 (2005 and 2009)	
VHDL IEEE 1076 (1987, 1993, 2002 and 2008)	
<b>RULE LIBRARIES</b>	
<b>ALDEC_BASIC (VHDL and Verilog)</b> <i>Basic rules to prevent simple coding mistakes (naming, style, formatting, etc.)</i>	
<b>ALDEC_RESTRICTIONS (VHDL and Verilog)</b> <i>Strongly recommended rules aimed to avoid harmful chip defects.</i>	
<b>CORE MECHANISMS</b>	
<b>Clocks and Resets Auto-detection</b> <i>Design control signals are detected automatically based on direct connections to clock/reset pins and propagation through different generation schemas.</i>	
<b>Reading and Generating SDC™ Constraints</b> <i>ALINT-PRO can suggest constraints based on the design analysis and considers constraints specified by the user.</i>	

Feature	Additional License Part
<p><b>Design Constraints Extension for IP Description</b>  <i>Aldec extension for design constraints to provide the tool with information about units without RTL description.</i></p>	
<p><b>FPGA Vendor Library Components Support (Xilinx, Intel, Microsemi, Lattice)</b>  <i>Components from popular FPGA vendor libraries are described with block-level constraints and are properly processed by all mechanisms.</i></p>	
<p><b>Incremental Design Entry and Hierarchical Constraints Promotion</b>  <i>Saving performance on secondary runs by re-using previous up-to-date outputs and replacing verified blocks with properly constrained stubs.</i></p>	
<p><b>Finite State Machines (FSM) Extraction from RTL</b>  <i>Recognition of FSM circuits along with their properties to verify a set of dedicated rules.</i></p>	
<p><b>Unit and Full Mode Linting</b>  <i>Two different linting methodologies that complement each other and are usually applied at different stages of the design cycle.</i></p>	
<p><b>Case Analysis</b>  <i>Ability to consider isolated modes of multi-mode circuits.</i></p>	
<p><b>Auto-build Black Boxes for Missing HDL Design Units</b>  <i>Automatic inference of black box units based on instantiations.</i></p>	
<p><b>Auto-deduce Timing Properties of Black Box Pins</b>  <i>Drafts of block-level constraints based on pure topology using clock/reset properties of connected nets.</i></p>	
<b>DEBUG CAPABILITIES</b>	
<p><b>Violation Viewer</b>  <i>Displays linting results presented in form of hierarchical tree and provides various debug options (such as cross-probing, waiving, etc.)</i></p>	
<p><b>Waiver Editor</b>  <i>Provides means to manage violations relevance using flexible waivers mechanism.</i></p>	

Feature	Additional License Part
<b>Configurable Reports (TXT, CSV, HTML, PDF)</b> <i>Dumping design analysis results in different formats with a large set of filters.</i>	
<b>TCL-based API to Linting results</b> <i>Custom template of violations report defined via TCL script that uses a set of built-in variables.</i>	
<b>Clocks and Reset Viewer</b> <i>Displays list of clocks and resets along with paths of their propagation in the design and provides cross-probing options.</i>	
<b>FSM Viewer and FSM Graph</b> <i>Dedicated tools for state machines analysis presenting FSMs in tree-like and graphical forms.</i>	
<b>RTL Schematic</b> <i>Displays graphical view of a design netlist and provides large set of navigation options.</i>	SCHV required
<b>Controls Schematic</b> <i>Displays a schematic-like representation of the clock/reset connectivity without unrelated elements.</i>	SCHV required
<b>DESIGN ENTRY AND MANAGEMENT</b>	
<b>Importing Active-HDL™, Riviera-PRO™, Vivado®, ISE®, and Quartus® Projects</b> <i>Automatic conversion of external designs into ALINT-PRO format (including support of Xilinx Out-of-Context IPs and Coregen blocks).</i>	
<b>File Browser</b> <i>Provides navigation throughout design resources stored on disk.</i>	
<b>Project Manager</b> <i>The tool for viewing and managing projects, workspaces and their associated items.</i>	
<b>Library Viewer</b> <i>Displays available libraries with their contents and allows managing libraries visibility.</i>	
<b>Elaboration Viewer</b> <i>Displays the design hierarchy tree.</i>	

Feature	Additional License Part
<b>Policy Editor</b> <i>Provides controls to manage requirements to be verified during the design linting.</i>	
<b>Flow Manager</b> <i>Tool to manage design analysis process that provides quick access to the main actions and displays status of their execution.</i>	
<b>Tasks Management</b> <i>Ability to create custom tasks associated with the design and to trace their implementation.</i>	
<b>SUPPORTED PLATFORMS</b>	
Linux® (32/64-Bit)	
Windows® 10/8.1/8/7 (32/64-Bit)	

## CDC Extension (LCDC)

Installed by main installation program. Additional installer should be used for ALDEC\_CDC rule library.

Feature	Additional License Part
<b>RULE LIBRARIES</b>	
<b>ALDEC_CDC (VHDL, Verilog, and SystemVerilog)</b> <i>Rules for CDC and RDC verification aimed to avoid metastability issues in complex designs.</i>	
<b>CORE MECHANISMS</b>	
<b>Clock Domains and Asynchronous Clock Groups Extraction</b> <i>Detecting groups of clocks synchronous to each other, forming corresponding domains and distributing sequential elements among them.</i>	
<b>Asynchronous Reset Domains Extraction</b> <i>Grouping sequential elements according to their asynchronous reset signals.</i>	
<b>Recognizing Clock and Reset Domain Crossings (CDC, RDC)</b> <i>Detection of signals that cross clock/reset domain boundaries and require appropriate synchronization.</i>	
<b>Multi-mode CDC Analysis (Consolidated, Case-based)</b> <i>By default, CDC paths are consolidated throughout all possible design operation modes. Individual modes can be analyzed separately as well.</i>	
<b>Synchronizers Patterns Recognition</b> <i>Typical synchronization circuits used in both FPGA and ASIC designs are supported and properly considered during the CDC analysis.</i>	
<b>Custom Synchronizers Description</b> <i>Constraints to instruct the product which custom circuit to treat as a synchronization one.</i>	

Feature	Additional License Part
<b>CDC Testbench Generation</b> <i>Provides CDC assertions, coverage statements for crossings and metastability insertion for CDC-aware simulation.</i>	
<b>DEBUG CAPABILITIES</b>	
<b>CDC and RDC Reports (TXT, CSV)</b> <i>Dump of all CDC and RDC related information, especially convenient for batch mode analysis.</i>	
<b>CDC Viewer</b> <i>Displays clock domains, their crossings, and synchronizers and provides cross-probing options.</i>	
<b>RDC Viewer</b> <i>Displays reset domains, their crossings, and synchronizers and provides cross-probing options.</i>	
<b>CDC Schematic</b> <i>Presents logical structure of the design suitable for analysis of CDC issues.</i>	SCHV required

## Schematic Windows (SCHV)

Installed by main installation program.

Feature	Additional License Part
<b>RTL Schematic</b> <i>Displays graphical view of a design netlist and provides large set of navigation options.</i>	
<b>Controls Schematic</b> <i>Displays a schematic-like representation of the clock/reset connectivity without unrelated elements.</i>	
<b>CDC Schematic</b> <i>Presents logical structure of the design suitable for analysis of CDC issues.</i>	LCDC required

## Optional Rule Libraries

Each rule library requires a separate installer and license part.

Rules Library	Additional License Part
ALDEC_PREMIUM (VHDL and Verilog)	LPREM
ALDEC_SV (SystemVerilog design subset)	LSV
DO-254 VHDL	LDO254-VHDL
DO-254 Verilog	LDO254-VLOG
STARC® VHDL	LSTC-VHDL
STARC® Verilog	LSTC-VLOG
RMM (VHDL and Verilog)	LRMM



## Rule Libraries Comparison

### Coverage of design areas - VHDL

	ALDEC_BASIC	ALDEC_PREMIUM	STARC_VHDL	DO254_VHDL	RMM	ALDEC_CDC
Plug-ins	ALDEC_BASIC_VHDL ALDEC_BASIC_PROJECT ALDEC_RESTRICTIONS	ALDEC_PREMIUM_VHDL ALDEC_PREMIUM_NETLIST	STARC_VHDL STARC_NETLIST STARC_PROJECT	DO254_VHDL DO254_NETLIST	RMM_VHDL RMM_NETLIST	ALDEC_CDC
naming conventions	22	4	37	2	26	7
readability, coding style	32	5	34	5	20	-
synthesis	14	8	92	31	11	-
FSM	2	17	8	-	4	-
design partitioning	-	14	4	-	2	-
simulation	2	2	9	2	-	-
clock, reset	-	11	19	11	9	29
CDC	-	1	5	-	-	16
constraints	-	-	-	-	-	6
DFT	-	-	28	-	-	-
performance, reuse	1	1	5	-	4	-
project organization	4	-	1	-	1	-
<b>Total</b>	<b>77</b>	<b>63</b>	<b>242</b>	<b>51</b>	<b>77</b>	<b>58</b>

## Coverage of design areas - Verilog/SystemVerilog

	ALDEC_BASIC	ALDEC_PREMIUM	STARC_VLOG	DO254_VLOG	RMM	ALDEC_CDC	ALDEC_SV
Plug-ins	ALDEC_BASIC_VLOG ALDEC_BASIC_PROJECT ALDEC_RESTRICTIONS	ALDEC_PREMIUM_VLOG ALDEC_PREMIUM_NETLIST	STARC_VLOG STARC_NETLIST STARC_PROJECT	DO254_VLOG DO254_NETLIST	RMM_VLOG RMM_NETLIST	ALDEC_CDC	ALDEC_SV
naming conventions	7	4	36	2	19	7	1
readability, coding style	14	5	35	8	12	-	32
synthesis	15	7	106	43	9	-	27
FSM	2	17	7	-	4	-	1
design partitioning	-	14	4	-	3	-	-
simulation	9	3	18	3	-	-	-
clock, reset	-	11	19	11	9	29	-
CDC	-	1	5	-	-	16	-
constraints	-	-	-	-	-	6	-
DFT	-	-	28	-	-	-	-
performance, reuse	-	1	1	-	2	-	-
project organization	3	-	1	-	-	-	-
<b>Total</b>	<b>50</b>	<b>63</b>	<b>260</b>	<b>67</b>	<b>58</b>	<b>58</b>	<b>61</b>