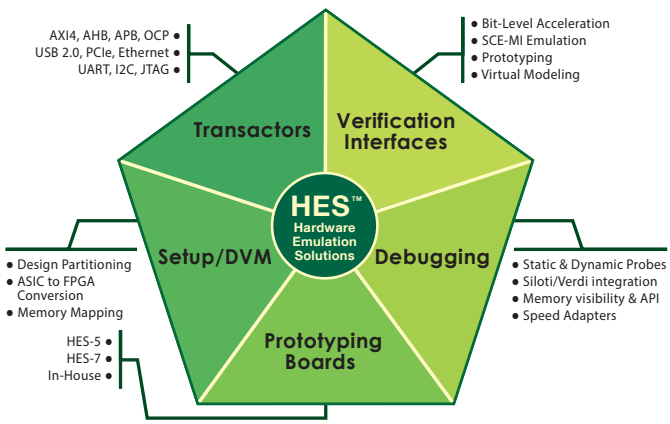
HES-DVM™ | HW/SW Validation Platform

Hybrid Verification Platform

HES-DVM™ is a Hybrid Verification and Validation Platform for Hardware and Software developers of SoC and ASIC designs up to 144M ASIC gates. Utilizing the latest in Xilinx® FPGA technology and the most up-to-date modeling interfaces for co-emulation, HES-DVM provides a high-speed emulation solution for pre-silicon test and debug with hardware speeds, real-time data interfaces, and an automated design environment. Partnered with Virtual Platform integration, API/ GUI interfaces for memory and signal debug, and a library of synthesizable peripheral transactors, design teams are able to reduce the verification cycle, increase throughput, and reduce overall costs.

Top Features

- **Bit-Level Simulation Acceleration**
- **SoC HW/SW Co-Verification**
- **Transaction Level Emulation with SCE-MI 2.1, SystemC/C/C++, TLM2.0**
- **Extensive Debugging (static/dynamic probes, memory access using GUI & API)**
- **Fully Scriptable Environment**
- **RTL Simulator Interfaces: Active-HDL™, NC-Sim®, ModelSim®, Riviera-PRO™, QuestaSim® and VCS-MX®**
- **Off-the-shelf FPGA prototyping boards support (Aldec HES-5, HES-7, and In-House Boards)**
- **Linux and Windows® XP/7/8 and 32/64 bit support**



Acceleration, Emulation, and Hardware Prototyping

HES-DVM enables hardware design teams with multiple modes of high-speed verification and validation including simulation acceleration, SCE-MI 2.1 emulation (Macro/ DPI Function based), and hardware prototyping for chip and system level verification of SoC and ASIC systems. Combined with fully integrated array of debugging tools allowing 100% visibility into the DUT and speed adapters to connect industry standard interfaces to the design environment, verification teams are able to reduce time and risks of silicon re-spins.

Software Development with Complete OS and Processor Solutions

Software developers today need early access to hardware to develop applications running on the latest OS in the newest embedded systems (e.g. ARM® Cortex). Utilizing Virtual Platforms with HES-DVM's Co-Emulation interface, developers are able to connect TLM modules to their hardware DUT via high speed AXI and AHB transactors. Partnering the design TB with HES-DVM memory management API, developers are able to load applications to program memory, decreasing overall system boot-time.

HES™ BUNDLE PACKAGES

Prototyping

DVM-PROTO Base Package

- Prototyping Mode
- Daughterboard Connection
- Manual Design Partitioning
- Linux and Windows® XP/7/8 and 32/64 bit support
- Hardware Boards Interface
- Prototyping API and function library
- Prototyping Testbench Co-Simulation Interface

Optional Proto Extensions

- Multiple-FPGA Board Support

Acceleration

DVM-XL Base Package

- Acceleration Mode
- Daughterboard Connection
- Manual Design Partitioning
- Linux and Windows® XP/7/8 and 32/64 bit support
- Hardware Boards Interface
- Automatic Design Partitioning
- User Directed Partitioning
- Black-Box Functionality
- Mirror-Box Functionality
- Clock Conversion and Analysis
- Static Debugging Probes
- Memory Model Mapping
- SystemC/C/C++ Testbench Wrapper for Acceleration
- Multiple-FPGA Board Support
- HDL Co-Simulation Interface

Optional XCELL Extensions

- Memory Viewer

Emulation

DVM-EMU Base Package

- Emulation Mode
- Daughterboard Connection
- Manual Design Partitioning
- Linux and Windows® XP/7/8 and 32/64 bit support
- Hardware Boards Interface
- Automatic Design Partitioning
- User Directed Partitioning
- Clock Conversion and Analysis
- Static Debugging Probes
- Emulation Results Stored in Waveform
- Memory Model Mapping
- SCE-MI Hardware/Software Infrastructure
- Memory Viewer
- Dynamic Debugging in SCE-MI
- Virtual Platform Processors
- Advanced Logic Analyzer

Optional EMU Extensions

- Processor Support
  - ARM 7/9/Cortex
  - Tensilica (Cadence)
  - Andes Tech

Elite

DVM-Elite Base Package

- Acceleration, Emulation, and Prototyping Mode
- Daughterboard Connection
- Manual Design Partitioning
- Linux and Windows® XP/7/8 and 32/64 bit support
- Hardware Boards Interface
- Automatic Design Partitioning
- User Directed Partitioning
- Black-Box Functionality
- Mirror-Box Functionality
- Clock Conversion and Analysis
- Static Debugging Probes
- Emulation Results Stored in Waveform
- Memory Model Mapping
- SystemC/C/C++ Testbench Wrapper for Acceleration
- Server Farm Support for Design Setup
- SCE-MI Hardware/Software Infrastructure
- HDL Co-Simulation Interface
- Prototyping API and function library
- Prototyping Testbench Co-Simulation Interface
- Memory Viewer
- Dynamic Debugging in SCE-MI
- Advanced Logic Analyzer

Optional ELITE Extensions

- Processor Support
  - ARM 7/9/Cortex
  - Tensilica (Cadence)
  - Andes Tech

Hardware FPGA Board Support up to 144 Million ASIC Gates




HES-5, HES-7, or In-House FPGA Protoyping Boards

Optional SCE-MI Transactors

Bus Protocol Transactor Models Available
AHB (AMBA 2.0) OCP, Wishbone, AXI4 (AMBA 4.0), AXI3 (AMBA 3.0), AXI4-Lite (AMBA 4.0)

Peripheral Transactor Models Available
UART, I2C, I2S, JTAG, SPI, SDIO,USB 2.0

Networking Transactor Models Available
10/100/1000 Gigabit Ethernet

Video Transactor Models Available
CCIR656 Image Sensor, HDMI 1.2a Source and Sink 1080p60, HDMI 1.3a Source and Sink 2560x1600p60

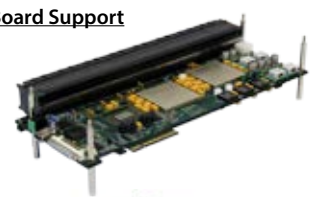
Serial Link Transactor Models Available
PCIe 2.0/1.1 endpoint, PCIe 2.0/1.1 rootport

MEMS Transactor Models Available
Accelerometer (G-Sensor), Gyrometer (Gyros)

Speed Adapter Models Available
SPI4.2, CSIX, PCIe Gen2, 1-wire, JTAG

FPGA Hardware Board Support

- **HES-5**
  HES5XLX220EX (1M ASIC Gate Capacity)
  HES5XLX660EX (4M ASIC Gate Capacity)
- **HES-7**
  HES7XV690BP (4M ASIC Gate Capacity)
  HES7XV1380BP (8M ASIC Gate Capacity)
  HES7XV2000BP(12M ASIC Gate Capacity)
  HES7XV4000BP (24M ASIC Gate Capacity
  Connect up to 6 HES-7 boards to support up to 144M ASIC Gates
- **In-House Prototyping Boards**




STANDARDS

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