Hybrid Verification Platform

HES-DVM™ is a hybrid verification and validation platform for hardware and software developers of SoC and ASIC designs. Utilizing the industry-proven co-emulation standards like SCE-MI or TLM and the newest Xilinx® FPGA technology, HES-DVM provides a high-speed emulation solution for pre-silicon test and debug with hardware speeds, real-time data interfaces, and an automated design setup environment. Partnered with HDL simulators, virtual platforms, hardware and software debuggers, and a library of synthesizable transactors and speed adapters, design teams are able to reduce the verification cycle and risks of silicon re-spins.

Top Features

- Scalable FPGA hardware platform utilizing the newest and largest Xilinx devices
- Versatile applications: Simulation Acceleration, Hybrid Co-Emulation, ICE, Physical Prototyping
- Transaction level standards support facilitating design of reusable transactors (SCE-MI, TLM)
- Extensive debugging with full visibility into FPGA and memory viewer
- Automated design setup with multi-FPGA partitioning and interconnections
- Patented clock conversion algorithm for reliable FPGA implementations and board-level timing closure
- Linux and Windows® environment support

Acceleration, Emulation, and Prototyping

HES-DVM combines high end FPGA prototyping boards utilizing newest and largest Xilinx FPGA chips with multiple modes of operation including Simulation Acceleration, Hybrid Co-Emulation, In-Circuit-Emulation and Physical Prototyping. High speed backplane solution makes the hardware scalable and appropriate for block level or chip level verification of SoC and ASIC designs. The functionality of hardware can be easily extended with reach choice of Daughter Cards making the HES-DVM platform the most versatile and cost effective on the market.

Software Development with Complete SoC and Hardware Prototype

Software developers today need an early access to the SoC hardware prototype to develop and debug applications that should be run on the latest OS or RTOS. Combining QEMU or Virtual Platform with HES-DVM, developers are able to connect virtual processor models with custom hardware RTL blocks using high speed bus transactors like AMBA AXI or AHB. Partnering such a hybrid hardware model with fully integrated array of debugging tools that enable full visibility, developers are able to load applications to program memory, decreasing overall system boot-time or check state of essential system registers directly in FPGA to validate required functionality or trace hardware related malfunctions.
## Standards

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## Partners

- **Aldec, Inc.**
- **Andes Technology**
- **ARM**
- **Helion**
- **Logicnorthwest**
- **Nexperia**
- **Xilinx**

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