RTAX/RTSX Adaptors

Frequently Asked Questions [FAQ]

Revision 1.8, March 10, 2021

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1 Power Supply Questions

Q1.1Are there any special requirements for Aldec Adaptor considering power supply voltages?

Aldec's RTAX/RTSX Adaptors are designed to be fully compatible with RTAX/RTSX powering systems so there are no other requirements than specified in Microchip's documentation.

Q1.2Are there any additional capacitors for decoupling needed?

RTAX/RTSX Adaptors are fully compatible with RTAX/RTSX power supply system and there is no need to add any additional capacitors on customer target board (there is no need to add more capacitors than required in Microchip's documentation).

Q1.3What is the power consumption of RTAX/RTSX Adaptor?

Power consumption depends on the target design loaded to A3PE chip and can be estimated using Microchip's power calculator available on Microchip website.
Exemplary power estimation is provided in Adaptor's technical specification (refer to “Power Estimation Example” chapter in technical specification for more details).

Q1.4Is it possible to power up the RTSX Adaptor without POWER_DB?

Yes, it is possible – in such case proper voltages should be delivered to power connector (refer to technical specification for detailed power connector pin mapping).

Q1.5Is there any power up voltage sequence required for RTAX/RTSX Adaptor boards?

No, there is no power up sequence required. Aldec's RTSX Adaptors are designed to be fully compatible with RTAX/RTSX powering systems so there are no other power requirements than specified in Microchips documentation – including power seqencing.

2 JTAG Interface, Programming / Configuration Questions

Q2.1: Does the RTAX/RTSX Adaptor need to be powered during programming/configuration process?

Yes, our Adaptors must be powered during configuration process. VJTAG, VCC and VPUMP must be supplied.

Q2.2: Can we power our test card safely where the ALDEC RTSX Adaptor board is installed, provided the device on the Adaptor board is still un-programmed?

There will some input signals of 5V present at I/Os - how long can the Aldec/test card be powered without programming without causing any damage? Do we need to take care for any unsuspected problems during first power up with unprogrammed device?

Aldec adaper board is able to handle described situation. Unprogrammed A3PE chip has IO buffers disabled with tri state High-Z state set. Additionally, Voltage level translator circuit separates 5V side from FPGA chip. Aldec Adaptor should work correctly from first power-up without any issues.

Q2.3: What is the recommended programmer used for A3PE chip programming?

The ProASIC3E chips on the Adaptor board should be programmed by JTAG connector using Microchip's FlashPro3 or FlashPro4 programmer.

Q2.4: Are the JTAG connector pins connected to dedicated JTAG pins of RTAX/RTSX?

RTAX/RTSX and ProAsic3E JTAG interfaces are separated. Configuring A3PE is possible only by JTAG connector on Adaptor's PCB, not on the customer board.

Q2.5: Why RTAX TDI and TDO pins are connected together?

RTAX TDI pin is connected to RTAX TDO pin to keep JTAG chain continuity on customer's board. A3PE's JTAG interface is available only on Adaptor's JTAG_CON connector (Adaptor's JTAG interface and JTAG chain on customer's board are separated). It makes A3PE's JTAG independent from other devices.

Q2.6: The schematic block diagram from technical specification shows that there is a 0Ohm resistor connecting TDO and TDI signals. Do I need to include it in my PCB layout?

The resistor is already on the Adaptor board.

Q2.7: What is JTAG_VPUMP pin for? Is there a specific value it needs to be driven?

VPUMP (charge pump voltage) is programming voltage for A3PE chip. This voltage can be driven by FlashPro programmer (FlashPro - 'Set Vpump' option in programmer settings should be ON) or can be driven externally. It should be in range: 3.15 V to 3.45V when programming FPGA and can be left floating during normal operation (not programming mode).

Q2.8: What should be the default state of J1 jumper (open or closed) during programming A3PE chip on RTSX Adaptors?

It should be closed by default.

Q2.9: What is the recommended part number for the right angle replacement for JTAG connector? (Only for CQ208-352 boards)

You can use simple 2x5 SMD connector in right angle option with 2.54mm pitch or Samtec connector with part number: TSM-105-01-T-DH.

Q2.10: What are the IOs state of unprogrammed A3PEchip?

If the device has never been programmed before, the I/Os are tri-stated.

Q2.11: What are the IOs state of A3PE chip during and after programming?

During programming the I/O state can be specified using the "Specify I/O states during programming" option available in Flashpro software. This can only guarantee the state till the device is programmed. Once programmed, the device I/O states are depended on the design logic.

3 IOs / Clocks / Dedicated Pins Functions Questions

Q3.1: RTAX Adaptor datasheet says that there are differential pair on your Adaptor board, can I still connect single-ended signals (clocks) to the Adaptor?

Yes, you can connect single-ended signals including clocks. The Adaptor supports both differential and single ended signals with controlled impedance.

Q3.2: Incorrect V_{OL} and V_{OH} voltage levels on IO lines (only RTSX Adaptors, rev. 2)

A possible reasons of incorrect V_{OL} and V_{OH} voltage levels are pull-down/pull-up resistors on IO lines on customer target board. ALDEC doesn't recommend having the external pull-up or pull-down resistors on IO lines. If pull-up or pull-down resistors are mandatory on customer target board, the resistor value should be over 50 kΩ. 50 kΩ is a safe recommended value - smaller pull-up or pull-down resistor is allowed only if the customer can accept higher V_{OL} or lower V_{OH}, the draft estimation is:
$V_{OL} = V_{CCOUT} \times 4.5k/(4.5k + R_{PU})$
$V_{OH} = V_{CCOUT} \times R_{PD}/(4.5k + R_{PD})$

Q3.3: Does the bidirectional level shifters takes care of issues related with powering up and direction selection by itself or do we need to follow any guidelines? (only RTSX Adaptors)

There is no need to configure bidirectional level shifters. All power supply and IO voltage levels conversions is handled automatically.

Q3.4: What are the unconnected VCCDA pins for?

Aldec Adaptors (based on A3PE FPGA chip) don't use VCCDA pins. Those pins have no effect on Adaptor's operations.
Please note that they should be connected considering to RTAX device's and your target design's requirements, to keep full functionality of your final design.

Q3.5: Why some of the RTAX clock globals are connected to to the quadrant clock lines. Is there any possibility to drive ProASIC3E globals from RTAX clock lines?

Because of reduced space on Adaptor's PCB we had to route some of RTAX clock lines to A3PE quadrant clock lines. It is possible to drive clocks from quadrant spines to global spines, but globals promotion using PDC constraint file is needed to do so.
Use "assign_global_clock -net name" PDC option (inside PDC file) for nets promoted to global net and "unassign_global_clock -net name" option for global clocks from netlist.
Please note, that router should be configured with "-promote_globals ON" parameter (it is OFF by default).
Please refer also to: “Global Promotion and Demotion Using PDC”, “Spine Assignment”, “Designer Flow for Global Assignment” sections from A3PE hand book, for more details about nets promotion.

Q3.6: Are there any IO termination requirements?

Aldec Adaptor is compatible with RTAX FPGA devices, so all inputs and outputs (even clocks) should be treated as RTAX inputs/outputs.

Q3.7: What is the maximum load which the levelshifter on RTSX adaptor board is able to drive ?

The levelshifter used on the adaptor board is able to drive capacitive loads of up to 70 pF.

Q3.8: What are input driver requirements for the RTSX adaptor's IOs? (only RTSX Adaptors)

For proper operation, the device driving the data I/Os of the RTSX adaptor board must have drive strength of at least ±2 mA.

4 Assembling / Soldering Questions

Q4.1: Are there any Soldering recommendations?

All recommendations are provided in Adaptor's technical specification.

Q4.2: Are there any Sockets for Aldec Adaptor Available?

No, we don't provide any socket for our Adaptors.

Q4.3: What is the melting point of solder type that was used to solder Microchip chip to the PCB?

Note: Aldec is in the process of migration of its products to lead-free technology. All the newest Aldec boards are RoHS compliant. Part of Aldec Adaptor boards that was assembled in leaded technology may be still availble on the market.

The metling point of the solder used to assembly the ProASIC chip to the Adaptor is 183°C (Pb/SN package) or 217°C (RoHS complaint lead-free package).

Q4.4: What is the peak temperature while soldering the Adaptor?

Note: Aldec is in the process of migration of its products to lead-free technology. All the newest Aldec boards are RoHS compliant. Part of Aldec Adaptor boards that was assembled in leaded technology may be still availble on the market.

The peak temperature during soldering process is 225°C for Pb/SN assembly or 245°C for Pb-Free assembly (refer to “Soldering Details” chapter from technical specification for more details).

Q4.5: What are suggested ways for unsoldering the Adaptor board?

To unsolder the Adaptor from the PCB the Hot Air or Infra Red methods can be used.

1) Hot Air method.

To use Hot Air method special nozzles are required. Hot air nozzle must be larger than Adaptor’s PCB to ensure hot air flow over flex frame solder joints. Hot Air Pencil can be used as well. The recommended heating process is a combination of preheat and top side heat.

2) Infra-Red method.

Unsoldering can be performed by Infra-Red tool. The recommended heating process is a combination of preheat and top side heat.

Notes:

- Unsoldering process should be preceded by preheating phase to temperature approximately 120ºC.
- All Aldec recommendations should be restricted during soldering/unsoldering process. (refer to “Soldering and Unsoldering Procedures for RTAX/RTSX Prototyping Adaptor” chapter from technical specification for more detailed description)
- Too high temperature or too long heating can damage the Adaptor board.

Aldec recommends to perform soldering and unsoldering by qualified assembly houses.

Q4.6: What are the holes in Adaptors PCB intended for?

Holes as well as fiducial points on the Adaptor are intended to assist the assembly process. They can be used for positioning of the Adaptor on your PCB.

Q4.7: What is the recommended preheat temperature before soldering/unsoldering process?

Soldering/Unsoldering process should be preceded by preheating phase to temperature approximately 120^{O}C. Too high temperature or too long heating can damage the Adaptor board. See all Aldec recommendations about soldering/unsoldering procedures in Adaptor's technical specifaction.

Q4.8: Do you have any information on forming and trimming the leads for CQFP packages?

CQFP leads of the adaptor board do not require trim and form process, they are already formed and have fixed dimensions.

Q4.9: What is the material composition of adaptor's BGA balls?

Note: Aldec is in the process of migration of its products to lead-free technology. All the newest Aldec boards are RoHS compliant. Part of Aldec Adaptor boards that was assembled in leaded technology may be still availble on the market.

Material composition of adaptor's solder balls is SAC305 (RoHS compliant lead-free technology) or SN63/Pb37 (leaded technology).

Q4.10: What is the CQ lead finish?

The plating on the pins are 100u" Ni underplate with 10u" of gold overplate.

5 Netlist Converter Questions

Q5.1: How to import converted EDIF, PDC files into the Microchip SoC Designer environment?

To implement converted project in the Microchip SoC Designer do the following:

- Create New Design in Designer.
- Select Proasic3E as Design Family
- Open Design Selection Wizard by **Tools -> Device Selection...**
- In the Design Selection Wizard select appropriate Die and Package (must be the same, as for adaptor board chip)
- Import converted EDIF and generated PDC file by **Files -> Import Source Files...**
- There can be also imported SDC template file to improve timing parameters of implemented design (for detailed description of timing improvements by SDC template file please refer to the RTAX2A3P_Converter_Appnote_HowToSpeedUpPostconversionProASIC3EDesign)
- Run Compilation and Layout

6 Other Questions

Q6.1: Timing parameters of the RTAX/RTSX Adaptor

ProAsic3E/Virtex-5 FPGAs and RTAX/RTSX FPGA chips are from different families. Becasue of that, design implemented into RTAX/RTSX chip may have a bit different timing parameters, than design implemented into Aldec's Adaptor boards.
Because of timing differences between A3PE and RTAX/RTSX families, Aldec Adaptor should be used more for functional testing than timing testig.

Q6.2: Is a global reset for ProASIC3 required?

There is no global reset pin for A3PE chip. As for the design, this is up to the customer how he handles that, reset signals can be mapped to external pins of ProASIC3 and Libero handles that. Dedicated global pins are available only for clocks.

Q6.3: What is the max RTSX Adaptors height?

ACT-RTSX board height is as below:
- 29mm - with Power DB installed (MB+DB)
- 13mm - without Power DB (MB only).

Q6.4: Can I use ACT-H3Ki-CQ352 for RTAX-4000S/SL chip?

ACT-H3Ki-CQ352 can't be used for RTAX-4000S/SL due to differences in pinout. For RTAX-4000S/SL ALEDC recommends to use ACT-H4Ki-CQ352 adaptor board (single board or two stacked can be used depending on the required capacity). Please refer to the table below for the complete list of supported FPGAs for each ALDEC adaptor board:

Table 1: The list of ALDEC RTAX/RTSX adptor boards

Adaptor Board Name	Chip on Adaptor Board	Supported FPGAs
RTAX-S/SL Family		
CQ208		
ACT-H600-CQ208	A3PE600-FG256	RTAX250S/SL-CQ208
CQ256		
ACT-H3Ki-CQ256	A3PE3000-2FG484i /-2FGG484i	RTAX2000S/SL-CQ256
CQ352		
ACT-H3Ki-CQ352	A3PE3000-2FGG484i	RTAX250S/SL-CQ352 RTAX1000S/SL-CQ352 RTAX2000S/SL-CQ352
ACT-H4Ki-CQ352	Up to 2x A3PE3000-2FGG484i	RTAX4000S/SL-CQ352(*)
CG624		
ACT-H3Ki-CG624	A3PE3000-2FGG896i	RTAX250S/SL-CG624 RTAX1000S/SL-CG624 RTAX2000S/SL-CG624
CG1152		
ACT-H2K-CG1152	XC5VLX330-2FF1760C /-2FFG1760C	RTAX2000S/SL-CG1152
CG1272		
ACT-H4K-CG1272	XC5VLX330-2FF1760C/ -2FFG1760C/ -1FFG1760i	RTAX4000S/SL-CG1272(**)
RTSX-SU/SX-A Family		
CQ208		
ACT-RTSXi-CQ208	A3PE600-2FGG484i	RTSX32SU-CQ208 RT54SX32S-CQ208 A54SX32A-CQ208
CQ256		
ACT-RTSXi-CQ256	A3PE600-2FGG484i	RTSX72SU-CQ256 RT54SX72S-CQ256 A54SX72A-CQ256
RTAX-DSP Family		
CQ352		
ACT-H4Ki-CQ352	Up to 2x A3PE3000-2FGG484i	RTAX2000D-CQ352(***) RTAX4000D-CQ352(*)(***)
CG1272		
ACT-H4K-CG1272	XC5VLX330-2FF1760C/ -2FFG1760C/ -1FFG1760i	RTAX2000D-CG1272 RTAX4000D-CG1272

(*) Before using ACT-H4Ki-CQ352 adaptor board in single ProASIC3E chip configuration for RTAX4000S/SL/D prototyping ALDEC recommends to verify if the design implements for single A3PE3000 chip

(**) ALDEC recommends to verify if the design implements for XC5VLX330 chip in ISE enviroment

(***) ALDEC recommends to verify if the design implements for A3PE3000 chip due to differences in architecture of ProASIC3E and RTAX-DSP FPGAs - refer to Q6.5 below.

Q6.5: Does Aldec ACT-H4Ki-CQ352 support RTAX-2000D and RTAX-4000D?

The ACT-H4Ki-CQ352 is designed to support RTAX-S/SL familily. The usage of this adapter for RTAX-DSP is possible - the pinout is the same but the diffrence in the resources of the ProASIC chip and RTAX-DSP is substantial - the ProASIC3e does NOT have the DSP silces.
ALDEC recommends verifying that the design implements into the ProAsic3 chip used on the adaptor board. Check imported RTL code or .edf netlist file from the Aldec netlist converter in the Microchip Libero environment. Run implementation for the ProASIC3E, (A3PE3000-2FGG484i). The result depends on how the customer is using the DSP functionality. If the results are acceptable, the ACT-H4Ki-CQ352 can be used.

Typical design flows are described below:

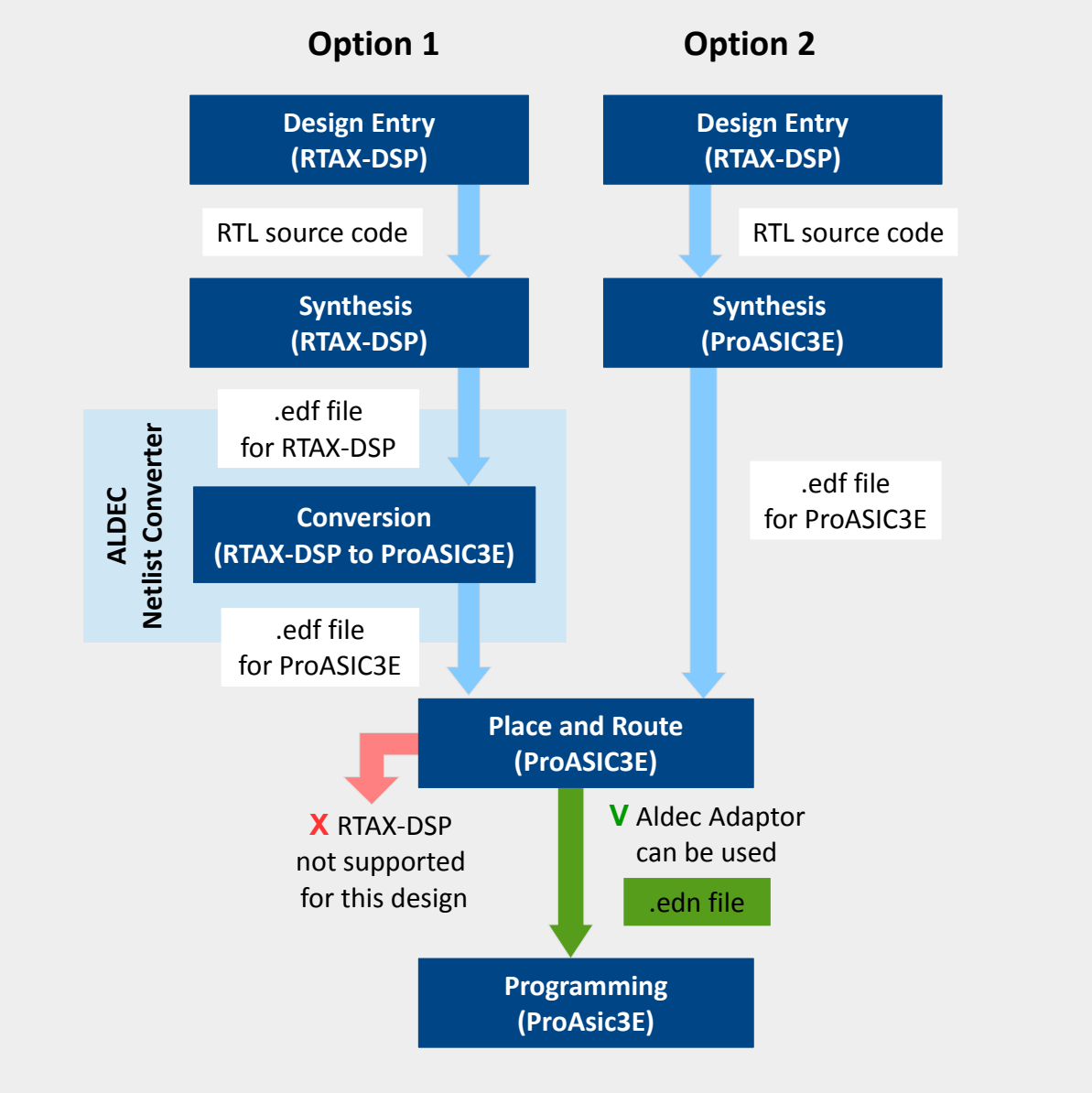

Figure 1. ACT-H4Ki-CQ352 – design flow for RTAX-DSP prototyping

Q6.6: Is there any quality control for the assembly of the adapter boards?

Adapter boards are checked for assembly quality and short circuits at subsequent stages of production by manufacturer.

All the adapter boards go through the following processes:

1. SMT
2. Reflow
3. Wash
4. Singulation
5. X-Ray
6. Connector Attach
7. Visual Inspection
8. AOI System for flatness and coplanarity inspection
9. Bakeout
10. QA Inspect
11. Final Pack

7 Programming with FlashPro - Known Issues

Q7.1: When user tries to program IDE 9.1 PDB file (PDB_VERSION : 1.7) using FlashPro 11.7 (or newer), it prompts an error message: "exit -10 failed to enable the FPGA array".

FLASHPRO ERROR MESSAGE:

programmer 'S201YPPR0A' : Scan Chain...
programmer 'S201YPPR0A' : Scan Chain PASSED.
programmer 'S201YPPR0A' : Executing action PROGRAM programmer 'S201YPPR0A' : EXPORT FSN[48] = 014a3150187c programmer 'S201YPPR0A' : Erase ...
programmer 'S201YPPR0A' : Completed erase programmer 'S201YPPR0A' : EXPORT CHECKSUM: [16] = 4b55 programmer 'S201YPPR0A' : Programming FPGA Array programmer 'S201YPPR0A' : Verifying FPGA Array
programmer 'S201YPPR0A' : Verifying FPGA Array -- pass
programmer 'S201YPPR0A' : Failed to enable FPGA Array.
programmer 'S201YPPR0A' : EXPORT ERROR_CODE[16] = 807b programmer 'S201YPPR0A' : Finished: Tue Aug 23 14:42:34 2016 (Elapsed time 00:01:47)
Error: programmer 'S201YPPR0A' : Executing action PROGRAM FAILED, EXIT 10, refer to FlashPro on-line help for details.

Workaround: There are multiple workaround for this:

1.Use STP file for programming .
2.Or Generate the programming file with Libero 11.7.
3.Or Program the PDB file with FlashPro 11.6
4.Or Launch FlashPro 11.7, Load 9.1 PDB , click on "Modify PDB" button and click OK. Now try to Program. It passes.

http://soc.microsemi.com/kb/article.aspx?id=KI8990

Q7.2: When user try to program with FlashPro5 programmer and old FlashPro version (up to v11.7) it prompts an error message: "VPUMP short detected"

FLASHPRO ERROR MESSAGE:

Error: programmer '03406' : Vpump short detected

"VPUMP short detected" error occurs regular with FlashPro5 programmer and old software version. This issue is fixed in the FlashPro version 11.8.

Workaround:

1.Use FlashPro version 11.8 or newer
2.Or use FlashPro4 programmer

8 Virtex-5 SPI Flash Programming - Known Issues

Q8.1: We have a problem with SPI FLASH memory programming. How to configure SPI memory chip?

Please follow below points:
1. Create the PROM file for the Flash memory that will be programmed through the FPGA, using instructions starting from page 7th (M25P128 PROM should be used):
http://www.xilinx.com/support/documentation/application_notes/xapp974.pdf
2. Folow procedure starting from page 13th (same document) - remember to select proper PROM chip (M25P128).
3. **Make sure that impact tool version is 13.4** - we have noticed that there are some issues with SPI PROM programming when using impact tool version 14.x. If you are using Windows8x64 or Windows 10 Operating System please refer also to Q8.3.

Q8.2: Error during Flash programming with Impact version 14.x

This is regular issue with Virtex-5 and Impact 14.x version. Please change the impact version on 13.4. If you are using Windows8x64 or Windows 10 Operating System please refer also to Q8.3.

Q8.3: Xilinx ISE/Impact 13.4 crashing on 'file open'.

This is a regular issue with Xilinx ISE 13.4 and OS Windows10 and Windows8x64. To fix it please follow the instructions below:

Rename libPortability.dll to libPortability.dll.orig, and copy libPortabilityNOSH.dll to libPortability.dll.
Do this in:
C:\Xilinx\13.4\ISE_DS\ISE\lib\nt64
C:\Xilinx\13.4\ISE_DS\common\lib\nt64 (copy dll from first location)

This will fix ISE and Impact crashes on file dialogs.
You may also run Xilinx ISE/Impact v13.4 on other the operating system.

Q8.4: What is the exact command to program SPI PROM and command to generate the MCS file?

Generate MCS file:
promgen -w -p mcs -c FF -o D:/simple -s 16384 -u 0000 D:/rtax2000/simple.bit -spi

Program PROM:
setMode -bscan
setCable -port auto
identify -inferir
identifyMPM
attachflash -position 1 - spi "M25P128"
assignfiletoattachedflash -position 1 -file "D:/cg1272_1252/simple.mcs"
program -p 1 -dataWidth 1 -spionly -e -v -loadfpga

Revision History Table

Date	Revision Number	Changes
March 8, 2021	1.8	- Added Question Q6.6 - Added FPGA PN option on CG1272 adapter board in Table 1 - Updated company name Microsemi/Actel on Microchip
December 3, 2020	1.7	- Added Chapter 8 “Virtex-5 SPI Flash Programming - Known Issues“
July 16, 2018	1.6	- Added Question Q3.7, Q3.8, Q4.10 - Added Chapter 7 “Programming with FlashPro - Known Issues“
April 28, 2017	1.5	- Added Revision History Table - Added Questions Q2.10, Q2.11, Q4.8 - Updated Q4.3, Q4.4, Q4.9, Q6.5 - Table 1 - ACT-H3Ki-CG624 board - added RTAX250S/SL-CG624 to supported FPGAs - Table 1 - Updated ProASIC3E part numbers with the RoHS compliant packages