# ALINT™ | Design Rule Checking

## Detects Design Flaws Early

Aldec's ALINT™ design analysis tool identifies critical design issues early in the design stage of ASIC and FPGA designs. The tool points out coding style, functional, and structural problems in Verilog®, VHDL, and mixed-language designs, preventing them from spreading to downstream stages of the design flow.

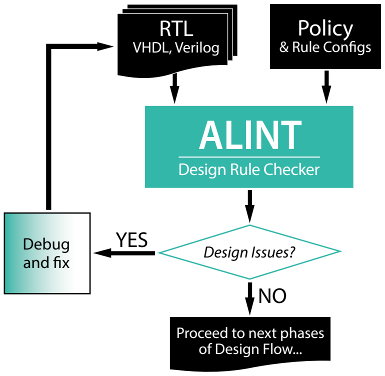
Sophisticated static analysis techniques uncover a variety of hidden bugs at the right time - when cost and efficiency of modifications are optimal, and highly reduce the risks of redundant design iterations and costly re-spins.

## Top Benefits

- **Design Flaws and Bugs are Detected During Early RTL Design Phase**
- **Phase-Based Linting Methodology: Guided Design Refinement Approach**
- **Industry-Leading Design Practices in STARC, RMM, and DO-254 Libraries**
- **Highly Customizable Framework for Rapid Automation of Design Expertise**
- **Integrated Debugging Environment for Convenient Results Analysis**
- **VHDL, Verilog®, and Mixed-Language Designs Support**
- **Linux and Windows® 7/Vista/XP/2003 32/64 Bit Support**
- **C++ Based API for Custom Rules Implementation**

## Methodology

ALINT leverages Phase-Based Linting (PBL) methodology to address the two most common problems with design rule checking tools; an excessive number of reports per session (common, as designs are checked against hundreds of rules) and a high level of "noise" caused by false or irrelevant violations. User productivity and overall efficiency of the entire linting process is significantly improved as PBL methodology puts clear priorities into the design refinement process and minimizes the number of iterations.



## Rule Libraries

ALINT's extensive design rule libraries are based on best practices, such as STARC and RMM, that have been established over the years by industry-leading companies in FPGA and ASIC design development. Libraries such as Aldec Basic and DO-254 capture the combined knowledge of Aldec customers and in-house design experts. The absolute majority of rules can be configured based on specific project needs. *C++ based API is also available and allows implementing fully custom and unique rules.*

## Framework

ALINT features customizable and intuitive framework that seamlessly integrates into existing environments and helps to automate design guidelines. Visual design management tools are integrated with the comprehensive knowledge base and provide an at-a-glance approach to capturing and execution of a company's own design expertise. Once the design rule checking policy customization and linting process execution is complete, the user may then take the benefits of the integrated debugging environment and its intuitive tools for detected design issues analysis and cross-probing between the violation reports and source code.

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ALDEC®
THE DESIGN VERIFICATION COMPANY

STANDARDS

IEEE

STARC

PARTNERS

achronix SEMICONDUCTOR CORPORATION

ALTERA

LATTICE

Microsemi

XILINX

| FEATURES | PRODUCT CONFIGURATIONS |
|---|---|
| **Supported Languages** | **ALINT** |
| Verilog® IEEE 1364 (1995, 2001 and 2005) | • |
| VHDL IEEE 1076 (1987, 1993, 2002 and 2008) | • |
| **Rule Libraries** | |
| Aldec Basic (VHDL and Verilog) | • |
| Aldec Premium (VHDL and Verilog) | Option |
| STARC® (VHDL or Verilog) | Option |
| DO-254 (VHDL or Verilog) | Option |
| RMM (VHDL and Verilog) | Option |
| User-Defined Rules | • |
| **Technology** | |
| Pattern Matching Engine | • |
| Instances Classification | • |
| FPGA Primitives Support | • |
| CDC Analysis and Reporting | • |
| **Design Refinement Methodology** | |
| Phase-Based Linting (PBL) | • |
| Flow Manager | • |
| Quality Scoring | • |
| Flow Editor | • |
| Critical Rules | • |
| **Results Analysis and Reporting** | |
| Standalone Reporting and Documentation | • |
| Violation Viewer | • |
| Exclusions Management | • |
| Cross Probing To Source Code | • |
| Violation Reports Comparison | • |
| **Productivity Tools** | |
| Design Management | • |
| Quick Launch Panel | • |
| Configuration Viewer | • |
| Rule Description Viewer | • |
| Rule Plug-in Viewer | • |
| Ruleset Editor | • |
| Rule Parameters Editor | • |
| Policy Editor | • |
| **Supported Platforms** | |
| Windows® 7/Vista/XP/2003 32/64 bit | • |
| Linux 32/64 bit | • |

## Practical Fields of Use

ALINT assists with all activities that take place during FPGA and ASIC design processes. All essential design objectives are addressed starting from the level of a new RTL block to system integration level when all blocks, including newly developed and existing ones, are put together.

## Development

At the level of new RTL development, ALINT verifies that all the essential design goals are achieved. Syntax and naming conventions start the list of conditions that must be met by a new RTL block. Subsequent checks answer important questions about whether the block will simulate and synthesize correctly. Once simulation and synthesis issues are cleared, mismatches between the RTL and gate-level simulations are then checked, and clocks and resets are validated for correct design.

## Reuse

When reusing existing components, it is important to ensure they are free from non-standard design techniques. A component structure is checked for adaptation issues – at this level it is important to ensure that reused code does not violate any critical rules that may have safety impact on the target design.

## Integration

At the system integration level, ALINT verifies that all individual blocks are implementation-ready and also checks for inter-block issues. The chip-level rules search for traceability of signals, indicate missing or incorrect synchronizers for signals that are transferred between different clock domains, point out scan chain management issues, and check many other design patterns.

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