ALINT-PRO™ | Design Rule Checking

Static Design Verification

ALINT-PRO™ is a static design verification solution for VHDL, Verilog, and SystemVerilog designs that uncovers critical design issues early in the design cycle without involving simulation. Running ALINT-PRO before RTL simulation and logic synthesis phases prevents design issues from spreading into the downstream stages of design flow and reduces the number of iterations required to finish the design.

ALINT-PRO™ covers a wide range of design issues including RTL and post-synthesis simulation mismatches, clock and reset trees analysis, clock domain crossings, proper design partitioning, DFT verification, design coding for reuse and portability, and many more.

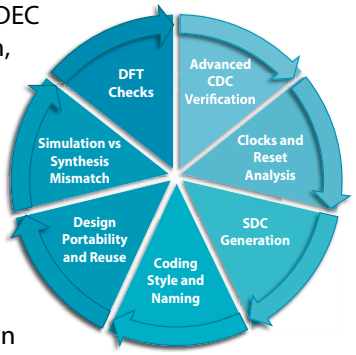
Key Benefits/Top Features

- **Static Design Verication** – performs analysis based on RTL and SDC sources and does not require complicated setup
- **DO-254 Support** – includes dedicated ruleset for safety critical designs to achieve compliance with DO-254 guidelines
- **Schematic Visualization** – ecient issues analysis, violated paths representation in graphical form and clock domains highlight
- **CDC Verication** – obtain all RTL and CDC checks in the same product with ALDEC_CDC rule plug-in and achieve best possible linting results
- **DFT Verication** – check for clock and reset controllability from external ports in the RTL design stage
- **Design Constraints** – easy design setup (reuse of existing constraint les), facilitate initial design constraints le creation
- **Design Constraints Extension** – increase analysis quality by proper verication of IP's, behavioral modules and black boxes

Industry Proven Guidelines

ALINT-PRO supports rule checks based on STARC (Semiconductor Technology Academic Research Center) and RMM (Reuse Methodology Manual) guidelines to utilize best practices in design development used by major semiconductor companies.

For safety critical designs, ALDEC offers DO-254 rule plug-in, focused on design stability, and is recommended to help achieve design compliance with the DO-254 standard.



ALDEC Basic and Premium rule plug-ins capture the combined knowledge of Aldec customers and in-house design experts and can supplement the above plug-ins, while ALDEC SV plugin targets new varieties of RTL mistakes specific to SystemVerilog design subsets.

ALINT-PRO contains a powerful Policy Editor to quickly build an efficient rules configuration based on design needs.

CDC Verification

ALINT-PRO features an optional ALDEC_CDC rule plug-in, which enables the full power of Clock Domain Crossing (CDC) and RTL analysis in a single product. It enhances verification with dynamic checks based on assertions and metastability emulation and offers additional debug capabilities such as highlighting of clock domains in the Schematic Viewer, and navigating over the detected clock domain crossings and identified synchronizers.

DFT Verification

ALINT-PRO supports a dedicated set of rules to verify clock and reset controllability from external ports in the RTL design stage to make design testing easier on subsequent design stages.

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ALDEC
THE DESIGN VERIFICATION COMPANY

STANDARDS

IEEE

STARC

PARTNERS

achronix SEMICONDUCTOR CORPORATION

ALTERA

LATTICE SEMICONDUCTOR

Microsemi

XILINX

FEATURES	PRODUCT CONFIGURATIONS
Supported Standards	
Verilog® IEEE 1364 (1995, and 2001)	•
SystemVerilog® IEEE 1800 (2005 and 2009)	•
VHDL IEEE 1076 (1987, 1993, 2002 and 2008)	•
Rule Libraries	
ALDEC BASIC (VHDL and Verilog)	•
ALDEC PREMIUM (VHDL and Verilog)	ALDEC PREMIUM Option
ALDEC SV (SystemVerilog Design subset)	ALDEC SV Option
STARC (VHDL and Verilog)	STARC VHDL/VLOG Option
DO254 (VHDL and Verilog)	DO254 VHDL/VLOG Option
ALDEC CDC (VHDL, Verilog, and SystemVerilog)	ALDEC CDC Option
Core Mechanisms	
Clocks and Resets Auto-detection	•
Clock Domains and Asynchronous Clock Groups Extraction	•
Metastability Insertion for CDC-aware Simulation	ALDEC CDC Option
CDC Assertions Generation	ALDEC CDC Option
Coverage Statements for Crossings	ALDEC CDC Option
Reading and Generating SDC Constraints	•
FPGA Vendor Library Components Support	•
Combinational Feedbacks Detection	•
Custom Synchronizers Description	•
DFT Checks	STARC VHDL/VLOG Option
Debug Capabilities	
RTL Schematic Viewer and Control Schematics	Schematics Option
Clocks and Resets Viewer	•
Elaboration Viewer	•
Violation Viewer and Tasks Management	•
Exporting Violation Reports (TXT, CSV, HTML, PDF)	•
CDC Viewer	ALDEC CDC Option
CDC Schematics	ALDEC CDC + Schematics Option
Design Management	
Project Manager	•
File Browser	•
Flow Manager	•
Library Manager	•
Policy Editor	•
Waiver Editor	•
Active-HDL, Riviera-PRO, ALINT, Vivado, ISE, and Quartus Projects	•
Supported Platforms	
Windows® 10/8.1/8/7 32/64 bit	•
Linux 32/64 bit	•

Design Constraints Setup

ALINT-PRO can read existing SDC™ constraint files previously created for synthesis and static timing analysis tools. The tool can also automatically generate initial SDC templates based on the topological analysis, including definitions of master and generated clocks, I/O delays, and asynchronous clock groups.

Design Constraints Extension

ALINT-PRO offers a custom extension to design constraints, an easy to read and straightforward format of block-level constraints to describe non-synthesizable behavioral modules, IP modules with protected code, vendor library cells, etc. Using constraints to describe a module's interface substitutes the black boxes in the netlist with equivalent models, which enable precise linting. It is also possible to describe designer's intent on reset controls, custom synchronization cells, and safe CDC paths, including paths with quasi-static sources.

Framework

ALINT-PRO provides a well-designed and tightly integrated GUI framework with intuitive interface and efficient issues analysis means. The Framework includes:

Schematic Viewer – offers graphical representation of a full synthesized netlist and violated paths highlighting, and clock domains highlighting. Control Schematics graphically demonstrates the relations between clocks and resets. CDC Schematics is a specialized visualization for domain crossings and synchronizers;
Clocks and Resets Viewer – shows clock and reset networks with all pins and nets which they propagate through;
Violation Viewer – enables violations filtering by various criteria, adding waivers, cross-probing to HDL and Schematic, and gives access to summary data.

Active-HDL™, Riviera-PRO™, Vivado™ and Quartus™ projects can be automatically converted to ALINT-PRO format, significantly minimizing time required for design setup.

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