ALINT-PRO-CDC™ | CDC Verification

Clock Domain Crossing Verification

ALINT-PRO-CDC™ is a design verification solution from Aldec which enables verification of clock domain crossings and handling of metastability issues in complex, modern multi-clock designs. Metastability issues cannot be checked reliably during conventional RTL simulation and a specialized tool should be used. ALINT-PRO-CDC uncovers metastability related issues early in the design cycle and is highly recommended to achieve verification goals for designs with multiple clock domains.

ALINT-PRO-CDC offers a verification strategy comprised of three key elements: Static Structural Verification, Dynamic Functional Verification, and Design Constraints Setup.

Key Benefits/Top Features

Static Structural Checks – confirm proper synchronization and verify against best practices

Assertions and Coverage – automatically generated testbench to verify proper pulse capturing and testbench completeness

Netlist Visualization – efficient issues analysis, violated paths representation in graphical form

Metastability Insertion – allows revealing functional errors during regular RTL simulation

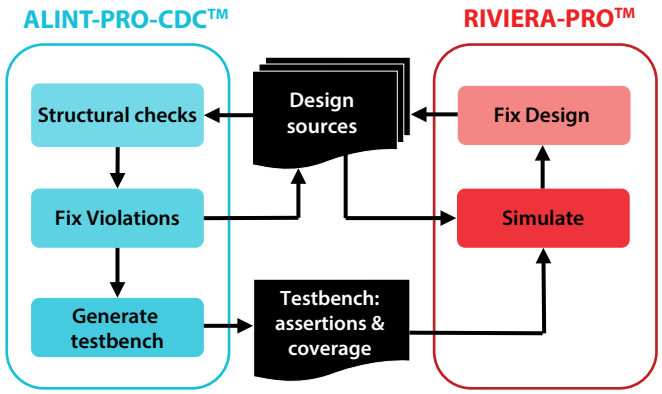
Design Constraints – easy design setup (reuse of existing constraint files), facilitate initial design constraints file creation

Design Constraints Extension – increase analysis quality by elimination of "holes" in the design and custom synchronizers support

Static Structural Verification

Static analysis includes detecting clock and reset networks, discovering combinational paths, extracting clock domains and crossings between them.

Clock and reset networks are checked to have proper connections in the design. The tool also reveals unconstrained clock sources, which allow existing SDC files verification for correctness. Crossings are checked to confirm proper synchronization and verified against best practices. Support is provided for NDFF, Pulse, MUX, and custom synchronizers.



Dynamic Functional Verification

Integration with Riviera-PRO™ simulator gives excellent verification quality by utilizing dynamic verification techniques together with static checks. Automatically generated SystemVerilog testbench inserts metastability emulation in the user's design and can be simulated together with original testbench. This enables metastability issues analysis in regular simulation-based verification flow. Testbench also includes assertions to verify data sent over domain boundaries captured by the receiving side. Coverage statements, provided by the testbench, help verify testbench completeness. They check that data transfers were triggered by the testbench and that delay, caused by metastability emulation, occurred both on signal transitions from Zero to One and from One to Zero.

STANDARDS

IEEE

STARC

PARTNERS

achronix

ALTERA

LATTICE

Microsemi

QuickLogic

tabula

XILINX

FEATURES	PRODUCT CONFIGURATIONS
Supported Standards	ALINT-PRO-CDC
Verilog® IEEE 1364 (1995, and 2001)	•
SystemVerilog® IEEE 1800 (2005 and 2009)	•
VHDL IEEE 1076 (1987, 1993, 2002 and 2008)	•
Rule Libraries	
ALDEC CDC (VHDL, Verilog, SystemVerilog)	•
Core Mechanisms	
Clocks and resets auto-detection	•
Clock domains extraction	•
Synchronizers patterns recognition	•
Metastability insertion	•
Assertion generation	•
Coverage statements for crossings	•
SDC generation	•
Vendor Library components support	•
Multiple drivers	•
Combinational feedbacks detection	•
Custom synchronizers description	•
Debug capabilities	
Schematic Viewer	•
Clocks and Reset Viewer	•
Hierarchy Viewer	•
Violation Viewer	•
HDL and Schematic cross-probing	•
Design Management	
Project Manager	•
File Browser	•
Quick Launch Panel	•
Library Manager	•
Policy Editor	•
Waiver Editor	•
Code Templates	•
Tasks Management	•
Active-HDL, Riviera-PRO, ALINT, Vivado, and Quartus projects conversion	•
Supported Platforms	
Windows® 8/7/Vista/XP/2003 32/64 bit	•
Linux 32/64 bit	•

Design Constraints Setup

ALINT-PRO-CDC can read SDC™ files for project configuration. This allows reusing existing configuration files for linting setup and makes it easier for the designer to work with the product.

The tool can automatically generate initial SDC file, which can be a good starting point for design configuration. Such files contain clocks declarations (create_clock/create_generated_clock constraints), and set_input_delay/set_output_delay constraints generated for top-level design ports based on the combinational paths analysis.

Design Constraints Extension

ALINT-PRO-CDC offers a custom extension to design constraints, an easy to read and straightforward format to describe non-synthesizable behavioral modules, IP modules with protected code, Vendor library cells, etc. Using constraints to describe module's interface substitutes black boxes in the netlist with equivalent models, which enable precise linting. It is also possible to describe custom synchronizer's interface with the help of constraints – such synchronizers are checked to be instantiated on crossings between asynchronous domains and that synchronized data is used in the destination domain.

Framework

ALINT-PRO-CDC provides a well-designed and tightly integrated GUI framework with intuitive interface and efficient issues analysis means. Framework includes Schematic Viewer – offers graphical representation of synthesized netlist and violated paths highlighting; Clocks and Resets Viewer – shows clock and reset networks with all pins and nets they are propagated through; Violation Viewer – enables violations filtering by various criteria, cross-probing to HDL and Schematic, and gives access to summary data.

Active-HDL™, Riviera-PRO™, ALINT™, Vivado™ and Quartus™ projects can be automatically converted to ALINT-PRO-CDC format, significantly minimizing time required for design setup.

Set of console commands provides rich scripting capabilities. Linting process is fully configurable from the console and can be adapted to user's needs.

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