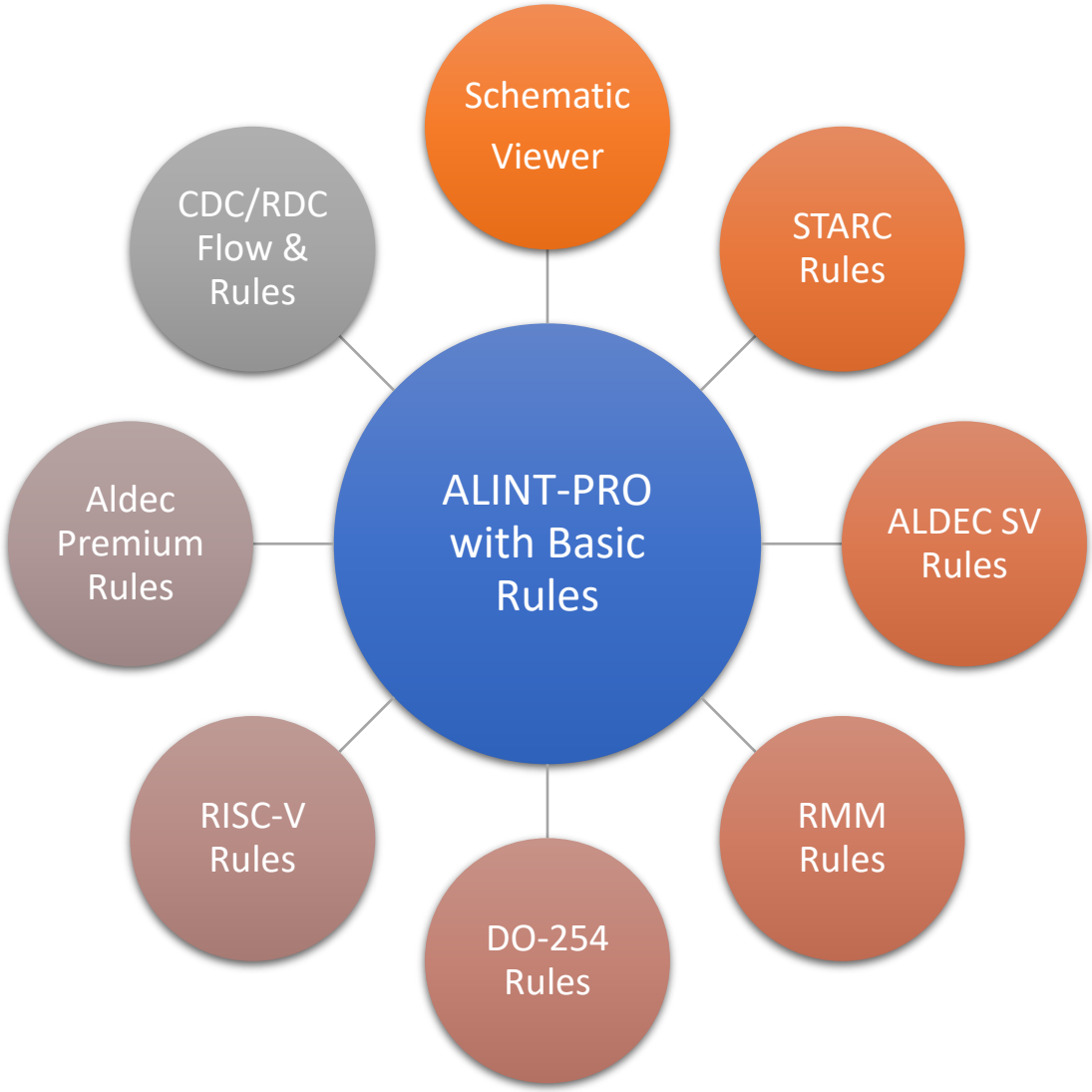

Aldec, Inc.
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Main Product (LNTPRO)

Installed by main installation program

Feature	Additional License Part
FRAMEWORK	
GUI, Interactive Console and Batch modes	
Macro, Tcl, Perl script support	
SUPPORTED STANDARDS	
Verilog® IEEE 1364 (1995, and 2001)	
SystemVerilog® IEEE 1800 (2005 and 2009)	
VHDL IEEE 1076 (1987, 1993, 2002 and 2008)	
RULE LIBRARIES	
ALDEC_BASIC (VHDL and Verilog) *Basic rules to prevent simple coding mistakes (naming, style, formatting, etc.)*	
ALDEC_RESTRICTIONS (VHDL and Verilog) *Strongly recommended rules aimed to avoid harmful chip defects.*	
CORE MECHANISMS	
Clocks and Resets Auto-detection *Design control signals are detected automatically based on direct connections to clock/reset pins and propagation through different generation schemas.*	
Reading and Generating SDC™ Constraints *ALINT-PRO can suggest constraints based on the design analysis and considers constraints specified by the user.*	

Feature	Additional License Part
Design Constraints Extension for IP Description *Aldec extension for design constraints to provide the tool with information about units without RTL description.*	
FPGA Vendor Library Components Support (Xilinx, Intel, Microsemi, Lattice) *Components from popular FPGA vendor libraries are described with block-level constraints and are properly processed by all mechanisms.*	
Incremental Design Entry and Hierarchical Constraints Promotion *Saving performance on secondary runs by re-using previous up-to-date outputs and replacing verified blocks with properly constrained stubs.*	
Finite State Machines (FSM) Extraction from RTL *Recognition of FSM circuits along with their properties to verify a set of dedicated rules.*	
Unit and Full Mode Linting *Two different linting methodologies that complement each other and are usually applied at different stages of the design cycle.*	
Case Analysis *Ability to consider isolated modes of multi-mode circuits.*	
Auto-build Black Boxes for Missing HDL Design Units *Automatic inference of black box units based on instantiations.*	
Auto-deduce Timing Properties of Black Box Pins *Drafts of block-level constraints based on pure topology using clock/reset properties of connected nets.*	
DEBUG CAPABILITIES	
Violation Viewer *Displays linting results presented in form of hierarchical tree and provides various debug options (such as cross-probing, waiving, etc.)*	
Waiver Editor *Provides means to manage violations relevance using flexible waivers mechanism.*	

Feature	Additional License Part
Configurable Reports (TXT, CSV, HTML, PDF) *Dumping design analysis results in different formats with a large set of filters.*	
TCL-based API to Linting results *Custom template of violations report defined via TCL script that uses a set of built-in variables.*	
Clocks and Reset Viewer *Displays list of clocks and resets along with paths of their propagation in the design and provides cross-probing options.*	
FSM Viewer and FSM Graph *Dedicated tools for state machines analysis presenting FSMs in tree-like and graphical forms.*	
RTL Schematic *Displays graphical view of a design netlist and provides large set of navigation options.*	SCHV required
Controls Schematic *Displays a schematic-like representation of the clock/reset connectivity without unrelated elements.*	SCHV required
DESIGN ENTRY AND MANAGEMENT	
Importing Active-HDL™, Riviera-PRO™, Vivado®, ISE®, and Quartus® Projects *Automatic conversion of external designs into ALINT-PRO format (including support of Xilinx Out-of-Context IPs and Coregen blocks).*	
File Browser *Provides navigation throughout design resources stored on disk.*	
Project Manager *The tool for viewing and managing projects, workspaces and their associated items.*	
Library Viewer *Displays available libraries with their contents and allows managing libraries visibility.*	
Elaboration Viewer *Displays the design hierarchy tree.*	

Feature	Additional License Part
Policy Editor *Provides controls to manage requirements to be verified during the design linting.*	
Flow Manager *Tool to manage design analysis process that provides quick access to the main actions and displays status of their execution.*	
Tasks Management *Ability to create custom tasks associated with the design and to trace their implementation.*	
SUPPORTED PLATFORMS	
Linux® (32/64-Bit)	
Windows® 10/8.1/8/7 (32/64-Bit)	

CDC Extension (LCDC)

Installed by main installation program. Additional installer should be used for ALDEC_CDC rule library.

Feature	Additional License Part
RULE LIBRARIES	
ALDEC_CDC (VHDL, Verilog, and SystemVerilog) *Rules for CDC and RDC verification aimed to avoid metastability issues in complex designs.*	
CORE MECHANISMS	
Clock Domains and Asynchronous Clock Groups Extraction *Detecting groups of clocks synchronous to each other, forming corresponding domains and distributing sequential elements among them.*	
Asynchronous Reset Domains Extraction *Grouping sequential elements according to their asynchronous reset signals.*	
Recognizing Clock and Reset Domain Crossings (CDC, RDC) *Detection of signals that cross clock/reset domain boundaries and require appropriate synchronization.*	
Multi-mode CDC Analysis (Consolidated, Case-based) *By default, CDC paths are consolidated throughout all possible design operation modes. Individual modes can be analyzed separately as well.*	
Synchronizers Patterns Recognition *Typical synchronization circuits used in both FPGA and ASIC designs are supported and properly considered during the CDC analysis.*	
Custom Synchronizers Description *Constraints to instruct the product which custom circuit to treat as a synchronization one.*	

Feature	Additional License Part
CDC Testbench Generation *Provides CDC assertions, coverage statements for crossings and metastability insertion for CDC-aware simulation.*	
DEBUG CAPABILITIES	
CDC and RDC Reports (TXT, CSV) *Dump of all CDC and RDC related information, especially convenient for batch mode analysis.*	
CDC Viewer *Displays clock domains, their crossings, and synchronizers and provides cross-probing options.*	
RDC Viewer *Displays reset domains, their crossings, and synchronizers and provides cross-probing options.*	
CDC Schematic *Presents logical structure of the design suitable for analysis of CDC issues.*	SCHV required

Schematic Windows (SCHV)

Installed by main installation program.

Feature	Additional License Part
RTL Schematic *Displays graphical view of a design netlist and provides large set of navigation options.*	
Controls Schematic *Displays a schematic-like representation of the clock/reset connectivity without unrelated elements.*	
CDC Schematic *Presents logical structure of the design suitable for analysis of CDC issues.*	LCDC required

Optional Rule Libraries

Each rule library requires a separate installer and license part.

Rules Library	Additional License Part
ALDEC_PREMIUM (VHDL and Verilog)	LPREM
ALDEC_SV (SystemVerilog design subset)	LSV
DO-254 VHDL	LDO254-VHDL
DO-254 Verilog	LDO254-VLOG
STARC® VHDL	LSTC-VHDL
STARC® Verilog	LSTC-VLOG
RMM (VHDL and Verilog)	LRMM
RISC-V (Verilog and SystemVerilog)	LRISCV

Rule Libraries Comparison

Coverage of design areas - VHDL

	ALDEC_BASIC	ALDEC_PREMIUM	STARC_VHDL	DO254_VHDL	RMM	ALDEC_CDC
Plug-ins	**ALDEC_BASIC_VHDL ALDEC_BASIC_PROJECT ALDEC_RESTRICTIONS**	**ALDEC_PREMIUM_VHDL ALDEC_PREMIUM_NETLIST**	**STARC_VHDL STARC_NETLIST STARC_PROJECT**	**DO254_VHDL DO254_NETLIST**	**RMM_VHDL RMM_NETLIST**	**ALDEC_CDC**
naming conventions	22	4	37	2	26	7
readability, coding style	32	5	34	5	20	-
synthesis	14	8	92	31	11	-
FSM	2	17	8	-	4	-
design partitioning	-	14	4	-	2	-
simulation	2	2	9	2	-	-
clock, reset	-	11	19	11	9	29
CDC	-	1	5	-	-	16
constraints	-	-	-	-	-	6
DFT	-	-	28	-	-	-
performance, reuse	1	1	5	-	4	-
project organization	4	-	1	-	1	-
Total	***77***	***63***	***242***	***51***	***77***	***58***

Coverage of design areas - Verilog/SystemVerilog

	ALDEC_BASIC	ALDEC_PREMIUM	STARC_VLOG	DO254_VLOG	RMM	ALDEC_CDC	ALDEC_SV	RISC-V
Plug-ins	**ALDEC_BASIC_VLOG ALDEC_BASIC_PROJECT ALDEC_RESTRICTIONS**	**ALDEC_PREMIUM_VLOG ALDEC_PREMIUM_NETLIST**	**STARC_VLOG STARC_NETLIST STARC_PROJECT**	**DO254_VLOG DO254_NETLIST**	**RMM_VLOG RMM_NETLIST**	**ALDEC_CDC**	**ALDEC_SV**	**RISCV**
naming conventions	7	4	36	2	19	7	1	0
readability, coding style	14	5	35	8	12	-	32	19
synthesis	15	7	106	43	9	-	27	46
FSM	2	17	7	-	4	-	1	10
design partitioning	-	14	4	-	3	-	-	-
simulation	9	3	18	3	-	-	-	-
clock, reset	-	11	19	11	9	29	-	3
CDC	-	1	5	-	-	16	-	-
constraints	-	-	-	-	-	6	-	-
DFT	-	-	28	-	-	-	-	-
performance, reuse	-	1	1	-	2	-	-	11
project organization	3	-	1	-	-	-	-	-
Total	***50***	***63***	***260***	***67***	***58***	***58***	***61***	***89***