Serial Front Panel Data Port is an industry standard, low-overhead, low-latency, high speed serial communications protocol. sFPDP is ideal for use in applications such as high-speed communication system backplanes, high-bandwidth remote sensor systems, signal processing, data recording, and high-bandwidth video systems. The simple and lightweight nature of the protocol makes it an attractive choice for replacement of parallel bus interconnects using serial transceiver technology. sFPDP can be used in point-to-point or loop topologies, uni-directional or bi-directional links, and easily supports different types of data with efficient and flexible data framing options.

StreamDSP is committed to performance, efficiency, and flexibility. Our sFPDP core is unique in that we support nearly all transceiver based devices from Altera and Xilinx. We’re always making improvements to the core with innovative new features such as multi-lane bonding for increased bandwidth, and we’re continually updating the core to support new transceiver based devices offered by both Altera and Xilinx. Our core provides a open interface to the FPGA transceiver, giving the user complete control over transceiver speed, settings and adjustments. A complete reference design is provided for each family, as well as a thorough testbench with support for Aldec’s Active-HDL and Riviera-Pro as well as Mentor’s ModelSim tools. In addition, our testing procedure includes exhaustive Altera <-> Xilinx interoperability testing to ensure compatibility.

StreamDSP is committed to delivering the highest level of customer support to ensure a smooth system integration. We also offer IP core customization and FPGA design services.
**Resource Usage**

<table>
<thead>
<tr>
<th>Registers</th>
<th>LUTs</th>
<th>*RAM</th>
</tr>
</thead>
<tbody>
<tr>
<td>772</td>
<td>841</td>
<td>14 Blocks</td>
</tr>
</tbody>
</table>

* RAM size dependent on user controlled TX and RX FIFO depths

**Throughput (per lane)**

<table>
<thead>
<tr>
<th>Line Rate</th>
<th>Throughput</th>
</tr>
</thead>
<tbody>
<tr>
<td>2.5 Gbps</td>
<td>247 MB/s</td>
</tr>
<tr>
<td>4.25 Gbps</td>
<td>420 MB/s</td>
</tr>
<tr>
<td>5.0 Gbps</td>
<td>494 MB/s</td>
</tr>
<tr>
<td>6.375 Gbps</td>
<td>630 MB/s</td>
</tr>
<tr>
<td>8.5 Gbps</td>
<td>841 MB/s</td>
</tr>
<tr>
<td>10.0 Gbps</td>
<td>990 MB/s</td>
</tr>
</tbody>
</table>

**FPGA Family Support**

**ALTERA**
- Cyclone-IV GX
- Arria GX
- Arria-II GX
- Arria-V GX
- Stratix-II GX
- Stratix-IV GX
- Stratix-V GX

**Example Design**
- Altera Cyclone-IV GX Starter Kit
- Altera Arria-GX PCIe Dev Kit
- Altera Arria-II GX PCIe Dev Kit
- Altera Arria-V GX PCIe Dev Kit
- Altera Stratix-II GX PCIe Dev Kit
- Altera Stratix-IV GX PCIe Dev Kit
- Altera Stratix-V GX PCIe Dev Kit

**XILINX**
- Spartan-6 LXT
- Kintex-7
- Virtex-4 FX
- Virtex-5 LXT
- Virtex-5 FXT
- Virtex-6 LXT
- Virtex-7

- Xilinx SP605 Development Kit
- Xilinx KC705 Evaluation Kit
- Xilinx ML405 Development Kit
- Xilinx ML555 Development Kit
- Xilinx ML507 Development Kit
- Xilinx ML605 Development Kit
- Xilinx VC707 Evaluation Kit

All deliveries include VHDL and Verilog simulation models, a self-checking testbench with simulation scripts, and ready-to-run design targeted at a popular development board for each family (listed above).