

- Achieves high clock rates with minimal routing constraints
- Supports quarter-rate clock operation
- Supports multi-bank refresh
- Supports multiplexed and non-multiplexed address interface to RLDRAM 3 devices
- Supports x18, and x36 devices in any combined data width (18, 36, 72, etc.)
- Multi-channel interface available where multiple requests can be accepted on each local clock
- Full run-time configurable timing parameters and memory settings
- Full set of Add-On Cores available
- Delivered fully integrated and verified with target DDR PHY
- Minimal ASIC gate count
- Broad range of ASIC and FPGA platforms supported
- Source code available
- Customization and Integration services available

The diagram illustrates the architecture of the Northwest Logic RDRAM 3 Controller. It is divided into two main sections: the controller logic and the external components.

Controller Logic (Northwest Logic RDRAM 3 Controller):

- Request Interface:** Receives external requests and sends them to the Request Buffer.
- Request Buffer:** Buffers requests, with data paths labeled $\times 1, \times 2$ and $\times 4$.
- Command Processing:** The central unit that receives requests from the buffer and sends commands to the PHY. It also receives status information from the Bank Status block.
- Bank Status:** Provides status information to the Command Processing unit, with a data path labeled $\times 16$.
- Control Blocks:** Initialization Control, Refresh Control, and ZQ Calibration Control. These blocks provide control signals to the Command Processing unit.

External Components and Interfaces:

- Command / Address / Control (DFI):** The interface between the Command Processing unit and the PHY.
- ASIC / Structured ASIC PHY:** The physical layer that handles the data transfer between the controller and the memory devices.
- RLDRAM 3 Device(s):** The external memory devices connected to the PHY.
- Data Interfaces:**
 - $I_{wr_data_chx}[2n-1:0]$: Write data bus.
 - $I_{wr_data_maskchx}[2m-1:0]$: Write data mask bus.
 - $I_{rd_data_chx}[2n-1:0]$: Read data bus.
- Configuration Ports:** Used for configuring the controller.
- clk:** Clock signal.
- reset_n:** Reset signal (active low).

Northwest Logic's Reduced Latency DRAM (RLDRAM) 3 Controller Core is designed for use in applications requiring high memory throughput, high clock rates and full programmability.

The core accepts commands using a simple local interface and translates them to the command sequences required by RDRAM 3 devices. The core also performs all initialization and refresh functions.

and its own soft DDR PHY. Contact Northwest Logic for more information.

Northwest Logic also provides IP Core customization services. Contact Northwest Logic for a quote.

- Core (Netlist or Source Code)
- Testbench (Source Code) with support for Aldec
- Complete Documentation
- Expert Technical Support & Maintenance Updates