OVERVIEW

The Genie-SSU USB 3.0 Verification IP Products are the industry’s most advanced verification solution for USB 3.0 based designs. The intelligent Verification Engine provides a full timing based bus functional model (BFM) for automatic constrained-random stimulus generation and protocol checking. It has a powerful Error Injector and extensive list of callbacks. A unique Interface Inspector provides the monitoring, checking, and scoreboard capability along with protocol compliance, functional coverage and error reporting. A comprehensive Compliance Suite is available with test cases for complete verification including corner cases which relieves engineers from the need to manually write tasks. This provides the Perfect combination of tools to ensure design success.

The Genie-SSU VIP provides a quick and efficient way to verify any USB 3.0 based design – Host, Device, Hub or PHY. It supports the USB 3.0 specification and tests all layer levels of the USB 3.0 design – PHY, Link and Protocol. Genie-SSU provides a complete verification solution that includes multi-language support and OVM and VMM methodology.

The Genie-SSU VIP provides:
- Bus Functional Models
- Protocol Checker
- Protocol Monitor
- Scoreboard
- Report Generator
- Error Injector
- Extensive Functional Coverage
- Callback Capability
- System level and block level testing
- Supports USB 3.0 PIPE ver. 1.0 specification
- Automatic /user configurable generation of flow control packets
- Configurable packet size for data packet payloads
- Supports all USB transactions: Control, Isochronous, Interrupt, Bulk and Bulk Streaming
- Supports randomization for all BFM Knobs and error injections
- Hub configuration support:
  - Packet generation directed for Hubs
  - LMP packet generation
  - Data transactions to device connected to Hub
  - Generation/storing of Hub specific descriptors
  - Control transactions specific to Hub
- Supports Loopback
- Supports LFPS signal generation and detection
- Supports UVM and OVM
- Easily integratable into any environment

FEATURES

- Complete Functional USB 3.0 Verification - Host, Device, Hub & PHY
- Compliant to USB 3.0 specification
- Operates at Super Speed USB rate of 5 GHz
- Automatic handling of Protocol, Link and PHY layer packets
- Full Link Training & Status State Machines (LTSSM)
- Automatic /user configurable generation of isochronous time stamp packets (host configuration)
- Automatic /user configurable generation of all LMP packets
- Supports Power Management:
  - Low power mode enable/disable (U1/U2)
  - Suspend (U3)
  - Active state (U0)
  - Resume/Remote Wakeup
- Configurable TS1, TS2, TSEQ, SKP ordered set generation
- Support for generation of all link commands
- Multiple Language Interface – SystemVerilog and Verilog
- Comprehensive Compliance Suite

Fig. 1: Example Device Design Verification

Fig. 2: Example Hub Design Verification
PRODUCT DETAILS

USB Host
The Genie-SSU Host VIP provides a full timing, bus functional model (BFM) that operates at 5 Gbps, SuperSpeed rates. The BFM initiates data transfer cycles and emulates the interface. The programmable Error Injector permits errors to be inserted at any layer of the protocol.

- Host performs bus enumeration and allocates independent USB pipes for communication flow
- Program TP sequences for Bulk, Isochronous, Interrupt, Bulk Stream, and Control transfer types

USB Device
Like the Genie-SSU Host, the Genie-SSU Device supports all the features and functions of the USB 3.0 device specification. Multiple instantiations of the device model can be configured in the simulation environment to connect to a USB hub design.

- Program USB Device requests to access USB device descriptors
- Support from 0 to N endpoints – each endpoint programmed separately
- Supports automatic response to all transaction types
- User configurable flow control – generation of ERDY and NRDY packets

USB PHY
Integrated into the Host and Device BFM, the USB PHY model provides accurate modelling at the serial or PIPE interface.

- Connect to RTL (MAC) on PIPE and PHY on serial side
- Clock and data recovery (SERDES)

BENEFITS
- Guarantees compliance to USB 3.0 specifications with ECN
- Enable faster testbench development and complete USB design verification
- Plug-and-play into all major simulation environments
- Ensure first pass design success
- Reduces risk to design flaws
- Reduces overall design and verification costs

<table>
<thead>
<tr>
<th>USB 3.0 COMPLIANCE SUITE</th>
<th>USB 3.0 SOLUTIONS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Developed by PerfectVIPs to thoroughly exercise USB 3.0 designs, the compliance suite is an advanced verification test suite that provides hundreds of test cases.</td>
<td>Developed by PerfectVIPs to address all USB 3.0 architectures, the following USB 3.0 SuperSpeed solutions are available.</td>
</tr>
<tr>
<td>- Verifies all layers of USB 3.0 designs</td>
<td>- Verification IP:</td>
</tr>
<tr>
<td>- Provides comprehensive design coverage targeted at Protocol, Link &amp; PHY layers</td>
<td></td>
</tr>
</tbody>
</table>
  - USB 3.0 Host VIP
  - USB 3.0 Device VIP
  - USB 3.0/2.0 Host VIP
  - USB 3.0/2.0 Device VIP
  - USB 3.0 Interface Inspector |
| - Unified customizable message formatting and reporting | Compliance Suites: |
| - Inject error at all layers |  
  - USB 3.0 Host Compliance Test Suite
  - USB 3.0 Device Compliance Test Suite
  - USB 3.0 Hub Compliance Test Suite |
| - Pre-built cover groups for functional coverage analysis | Supported Simulators |
| - Powerful and flexible pre-built OVM sequence libraries for generating test scenarios for coverage driven verification |  
  - Aldec, Cadence, Mentor and Synopsys |
| - Pre-built constraint library which allows constrained random stimulus generation ensuring robust verification |           |