OVERVIEW

The Genie-PCIe™ Verification IP Products provide the most robust verification solution for PCIe 3.0 based designs. The intelligent Verification Engine, advanced Interface Inspector and comprehensive Compliance Suite provide the Perfect combination of tools to reduce design risk, verification time and project costs. Genie-PCIe™ Verification IP also supports NVMe standard 1.0 & SR-IOV.

The Genie-PCIe™ VIP provides a quick and efficient way to verify any PCIe based design – Root Complex, End Point or Switch. It supports the PCIe 3.0 specification and is backwards compatible with PCIe 2.0, 1.1 and 1.0a specification addressing all layers of the PCIe protocol – Phy, Datalink, Transaction layer and Configuration Space. Genie-PCIe provides a complete verification solution that includes multi-language support and OVM/UVM methodology.

The Genie-PCIs VIP provides:
- Bus Functional Models
- Directed and Random Transaction Generator
- Packet & Order set Generator
- Error Injector
- Callbacks
- Monitor/Checker/Scoreboard
- Report Generator

FEATURES

- Compliant with PCI Express Specification v3.0, v2.0, v1.1 and 1.0a
- Link width support: x1, x2, x4, x8, x12, x16, x32
- Supports up to 8 virtual channels
- Verification at PIPE, 10b, and serial interface
- Supports randomization for packet fields and data payload with or without error injection
- Checks all TLPs for correct formation of headers, prefixes and ECRC
- Robust BFM API automates sending TLPs/DLLPs and controlling automatic BFM device response behaviour and link and device state transitions
- Generates message transfers
- Generates block read and write transfers to memory space and message transfers
- Generates message transfers
- Full Requester and Completer functions
- Supports OVM/UVM methodology
- Comprehensive Compliance Suite

- Supports 128b/130b (Gen 3) and 8b/10b (Gen 1/2) encoding
- Full LTSSM (Link Training & Status) support
- Complete Configurable Order Management logic
- Automatic /user configurable handling of all layer packets
- Automatic /user configurable generation of flow control packets and credit management
- Full DL state machines and configurable ACK/NACK and Replay timers
- Supports transaction-oriented request-completion and error injection sequences based on address and command type attributes
- Generates message transfers
- Supports Error Injection at all layers
- Supports Performance evaluations like bandwidth, utilization, efficiency calculations
- Supports ARI
- Language Interface – SystemVerilog & Verilog
- Supports NVMe
- Supports SR-IOV
**PRODUCT DETAILS**

**Single-Link Operation:** In the single-link mode, the BFM is configured as a single link supporting x1, x2, x4, x8, x12, x16 or x32 operation. The BFM is enriched with knobs to provide complete configurability over packet transmission and reception behaviour. Simple and easy APIs allow users to inject packets/errors at any layer.

**PCIe Coverage:** PCIe coverage gives a complete functional coverage with the facility to back track coverage holes back to specification section number, even line number.

**PCIe Checker:** PCIe checker provides bus-level protocol checking capability. It performs real-time reporting.

**PCIe Scoreboard**

 PCIe Scoreboard holds expected data and DUT data and does comparison.

**PCIe Interface Inspector:** The Interface Inspector tracks the traffic of the link and provides protocol-checking capability. Checks are configurable. They can be enabled and disabled individually for a particular test. It generates LOG file and displays protocol specific and transaction information. The log file can be tailored by the user depending on the requirement. Various verbosity levels are supported for warning, debug, errors and log.

The Genie-PCIe Interface Inspector checker provides protocol-checking capability with the following built-in rules:
- Endpoint rules
- Root Complex Integrated Endpoint Rules
- TLPS with Data Payloads Rules
- Routing and Addressing Rules
- First/Last DW Byte Enables Rules
- Memory, I/O & Configuration Request Rules
- Message Request Rules
- Completion Rules
- Request Handling Rules
- Completion Handling Rules
- Transaction Ordering Rules

**BENEFITS**

- Guarantees compliance to PCIe 3.0 specification
- Reduces test development effort
- Block level and System level verification
- Shortens verification schedule
- Reduces overall design and verification costs
- Plug-and-play into all major simulation environments

**SUPPORTED SIMULATORS: ALDEC, CADENCE, MENTOR, SYNOPSYS**

**PCIe 3.0 COMPLIANCE SUITE**

- Developed by PerfectVips, the compliance suite is a PCI-SIG based compliance test with additional compliance coverage from checklists.
- Verifies all layers of PCIe designs
- Provides comprehensive design coverage targeted at Phy, Data Link, Transaction & Configuration Space
- Identifies all protocol violations
- Provides detailed reports on functional coverage
- Provides directed and constrained random

**PCIe 3.0 SOLUTIONS**

- Developed by PerfectVips to address different system level PCIe architectures, the following PCIe solutions are available:
  - Verification IP:
    - PCIe 3.0 Root Complex (RC) VIP
    - PCIe 3.0 End Point (EP) VIP
    - PCIe 3.0 RC/EP VIP (configurable)
    - PCIe 3.0 RC Interface Inspector
    - PCIe 3.0 EP Interface Inspector

  Compliance Suites: