The solution from Creonic for data rates of up to 1 Gbit/s offers outstanding efficiency in terms of implementation complexity. Area and energy efficiency played a decisive role during the LDPC code design process. With this unified approach not only outstanding efficiency is obtained, but also excellent error correction performance, outperforming Viterbi decoders by up to 3 dB. At the same time, a throughput of hundreds of Mbit/s can be achieved even on low-cost FPGAs.

Benefits

- Decodes more than 5 codeword bits per clock cycle for throughputs beyond 1 Gbit/s.
- Gains up to 3 dB compared to Viterbi decoders.
- Low-power and low-complexity design.
- Layered LDPC decoder architecture, for faster convergence behavior.
- Block-to-block on-the-fly configuration.
- Early stopping criterion for iterative LDPC decoder, saving a considerable amount of energy.
- Configurable amount of LDPC decoding iterations for trading-off throughput and error correction performance.
- Collection of statistic information (number of modified information bits, number of iterations, decode success).
- LDPC encoder included.
- Available for ASIC and FPGAs (Xilinx, Altera).

Related Products

- 802.11n/ac LDPC Decoder
- 802.15.3c LDPC Decoder
- DVB-RCS2 Turbo Decoder
- DVB-S2 LDPC/BCH Encoder and Decoder
- DVB-C2 LDPC/BCH Decoder

Features

- Compliant with Multiband OFDM Physical Layer Specification, PHY Specification: Final Deliverable 1.5, August 11, 2009
- Support for all LDPC codes (approximate channel coding rates 1/2, 5/8, 3/4, 4/5)
- Support for short and long blocks (1,200 and 1,320 bits)

Applications

- Ultra-wideband (UWB)
- Wireless USB
- Microwave Links
- Optical Links
- TeleCare / TeleHealth
- Further High-throughput Applications

Deliverables

- VHDL source code or synthesized netlist
- HDL simulation models e.g. for Aldec’s Riviera-PRO
- VHDL or SystemC testbench
- bit-accurate Matlab, C or C++ simulation model
- comprehensive documentation
About Creonic

Creonic is an ISO 9001:2008 certified provider of ready-for-use IP cores for several algorithms of communications such as forward error correction (LDPC and Turbo coding), synchronization, and MIMO. The product portfolio covers standards like DVB-S2, DVB-RCS2, DVB-C2, WiFi, WiGig, and UWB. The products are applicable for ASIC and FPGA technology and comply with the highest requirements with respect to quality and performance. For more information, please visit www.creonic.com.

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