DVB-RCS (Digital Video Broadcast - Interaction channel for satellite distribution systems) is an established ETSI standard for digital data transmission via satellites. It uses a 8-state double-binary turbo decoder that has an excellent error correction performance. This outstanding performance of the DVB-RCS turbo decoder makes it the ideal candidate for further applications where high spectral efficiency is key for lowering costs.

Benefits

- Gains up to 4 dB compared to convolutional codes.
- Design-time configuration of throughput, input bit widths, and maximum block length for optimal resource utilization.
- Low-power and low-complexity design.
- Burst-to-burst on-the-fly configuration.
- Configurable interleaver parameters allow for support of custom block lengths.
- On-the-fly bit error rate measurement.
- High block length and code rate granularity.
- Configurable amount of turbo decoder iterations for trading-off throughput and error correction performance.
- Allows for easy migration from legacy DVB-RCS turbo decoders.
- Allows for turbo synchronization to further improve error correction performance (on request).
- Available for ASIC and FPGAs (Xilinx, Altera).

Performance Figures

- Payload throughput of up to 131 Mbit/s at 5 iterations and 82 Mbit/s at 8 iterations (200 MHz).
- BLER 10^{-5} with code rate 3/4 at
  - E_S/N_0 = 6.1 dB (QPSK, 53 payload bytes)
  - E_S/N_0 = 5.2 dB (QPSK, 212 payload bytes)

Features

- Compliant with ETSI 301 790 V1.4.1 (2005-09) (DVB-RCS)
- Support for all DVB-RCS payload block sizes (12 to 216 bytes) and code rates (1/3 to 6/7)
- Support for QPSK and 8-PSK modulation interfaces

Applications

- Satellite communication
  - Interactive Services
  - Professional Services
  - TDMA
- Applications with highest demands on forward error correction
- Applications with the need for a wide range of code rates (1/3 and above) and block lengths

Deliverables

- VHDL source code or synthesized netlist
- HDL simulation models e.g. for Aldec's Riviera-PRO
- VHDL or SystemC testbench
- bit-accurate Matlab, C or C++ simulation model
- comprehensive documentation

Related Products

DVB-RCS2 Turbo Decoder

DVB-S2 LDPC/BCH Encoder and Decoder

GEO-Mobile Radio LDPC Decoder

DVB-C2 LDPC/BCH Decoder

802.11n/ac LDPC Decoder

About Creonic

Creonic is an ISO 9001:2008 certified provider of ready-for-use IP cores for several algorithms of communications such as forward error correction (LDPC and Turbo coding), synchronization, and MIMO. The company offers the richest product portfolio in this field, covering standards like DVB-S2X, LTE-A, DVB-RCS2, DOCSIS 3.1, CCSDS, WiFi, WiGig, and UWB. The products are applicable for ASIC and FPGA technology and comply with the highest requirements with respect to quality and performance. For more information, please visit www.creonic.com.

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