DVB-RCS2 (Digital Video Broadcast - Second Generation DVB Interactive Satellite System) is the latest ETSI standard of the second generation for digital data transmission via satellites.

The Creonic DVB-RCS2 Multi-Carrier Receiver supports multiple frequency time domain multiple access (MF-TDMA), performs all tasks of an DVB-RCS2 receiver including carriers separation, baseband conversion, demodulation, and turbo decoding. It can process intermediate frequency (IF) real signal with center IF frequencies between 0 and 100 MHz. The Creonic turbo decoder is included in the receiver to provide users with Frame PDUs at the output.

Benefits

- Supports MF-TDMA using the DVB-RCS2 protocol.
- The receiver performs multi-carrier processing. including gain adjustment, timing correction, decimation, filtering, bursts synchronization, derotation, descrambling, phase and frequency correction, DVB-RCS2 deframing, turbo decoding, and CRC-16 / CRC-32 checks.
- On-the-fly reconfiguration of superframe and number of active carriers.
- Configurable amount of turbo decoder iterations.
- Low-power and low-complexity design.
- AXI4-Lite interface for controlling and for retrieving status information.
- Collection of statistics (error rates, superframe and timeslot counters, frequency and timing offsets, signal-to-noise ratio (SNR)).
- Validated on AMD Xilinx RFSoC board with the Creonic DVB-RCS2 modulator
- Available for ASIC and FPGAs (AMD Xilinx, Intel).

Key Features

- Supports 32 carriers at aggregate symbol rate of 50 MSymbols/s, sample rate of 200 MSamples/s.

Features

- Compliant with ETSI EN 301 545-2 (DVB-RCS2)
- Support for Linear Modulation Bursts of Table A-1
- Optional support for Spread-spectrum Linear Modulation Bursts waveforms of Table A-2
- Support for BPSK, QPSK, 8-PSK, 16-QAM
- Supports real, intermediate frequency signal at input.

Applications

- Satellite communication
  - Digital Video Broadcasting
  - Interactive Services
  - Professional Services
  - News Gathering

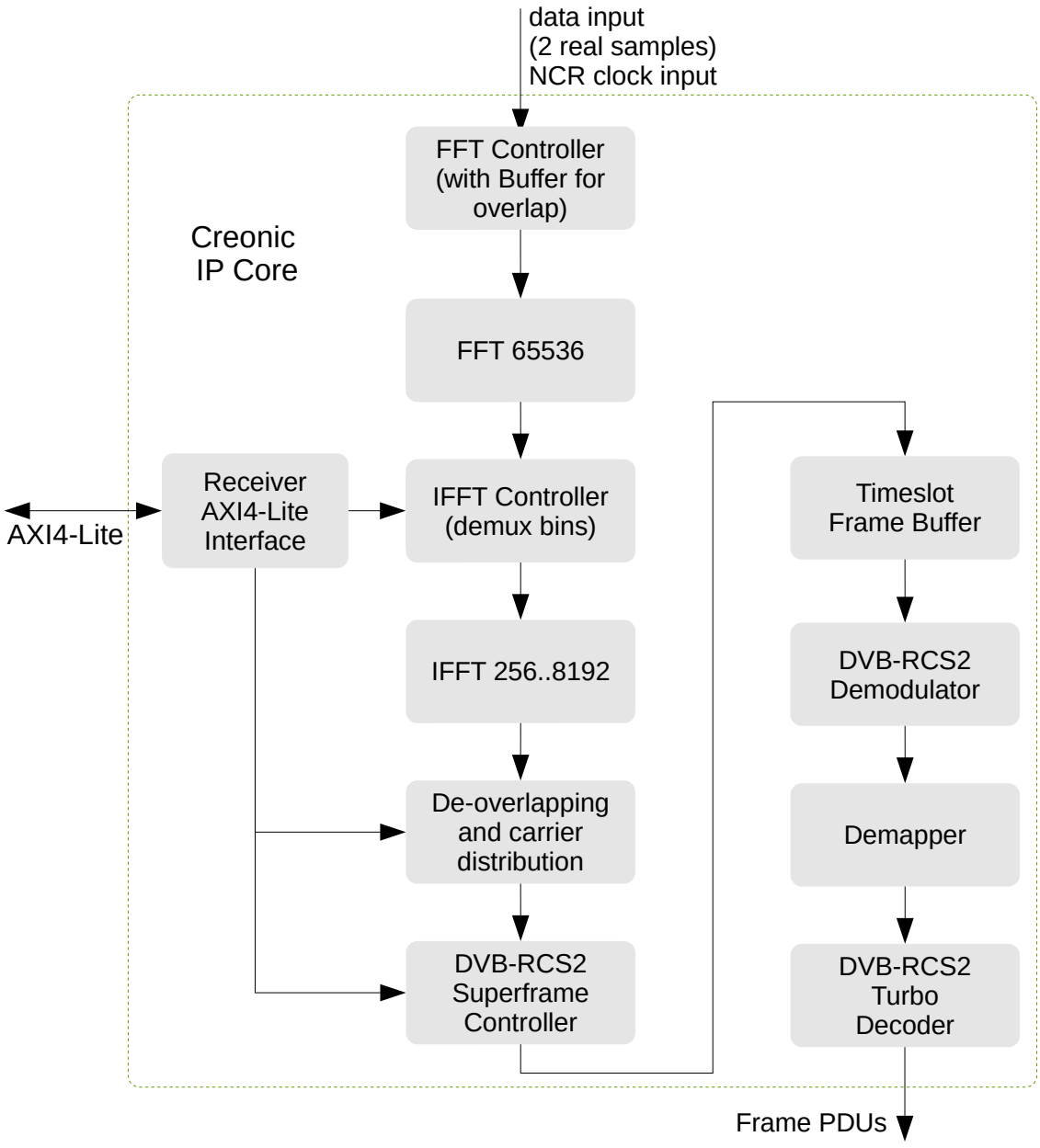
Deliverables

- VHDL source code or synthesized netlist
- HDL simulation models e.g. for Aldec's Riviera-PRO
- VHDL testbench
- bit-accurate Matlab, C or C++ simulation model
- Comprehensive documentation

- Supports symbol rate per carrier from 200 kSymbols/s to 12.5 MSymbols/s at an input rate of 200 MSamples/s.

DVB-RCS2 Multi-Carrier Receiver Overview

The following figure gives an overview of all components that are part of the DVB-RCS2 Multi-Carrier Receiver IP core. The receiver reads a quantized real signal from an analog digital converter (ADC) for processing. The FFT and IFFT stages separate the carriers and distribute them to RCS2 demodulator. After that the signal is demodulated and decoded by the integrated turbo decoder. The receiver provides the bytes of the Frame PDUs at the output. The user configures the receiver with an AXI4-Lite interface.


data input
(2 real samples)
NCR clock input
Creonic
IP Core
FFT Controller
(with Buffer for
overlap)
FFT 65536
Receiver
AXI4-Lite
Interface
AXI4-Lite
IFFT Controller
(demux bins)
IFFT 256..8192
De-overlapping
and carrier
distribution
DVB-RCS2
Superframe
Controller
Timeslot
Frame Buffer
DVB-RCS2
Demodulator
Demapper
DVB-RCS2
Turbo
Decoder
Frame PDUs

Related Products

DVB-RCS2 Modulator

DVB-RCS2 Turbo Decoder

DVB-S2X Demodulator

DVB-S2X LDPC/BCH Decoder

About Creonic

Creonic is an ISO 9001:2015 certified provider of ready-for-use IP cores for wired, wireless, fiber, and free-space optical communications. All relevant digital signal processing algorithms are covered, including, but not limited to, forward error correction, modulation, equalization, and demodulation. The company offers the richest product portfolio in this field, covering standards like 3GPP 5G, DVB-S2X, DVB-RCS2, CCSDS, and WiFi. The products are applicable for ASIC and FPGA technologies and comply with the highest requirements with respect to quality and performance. For more information please visit our website at www.creonic.com.

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