The Creonic CCSDS LDPC IP cores support the LDPC coding scheme as defined by the CCSDS standard. The LDPC code with single rate 223/255 was specifically designed for Near-Earth missions, but the excellent error correction performance also makes it an ideal solution for a wide variety of high-throughput applications. The IP cores are available for ASIC and FPGAs (AMD Xilinx, Intel, Microchip).

CCSDS LDPC Decoder

Key benefits of the decoder are:

- Gains of up to 3 dB compared to Viterbi decoders.
- Low-power and low-complexity design.
- Layered LDPC decoder architecture, for convergence behavior that is twice as fast as non-layered LDPC decoders.
- Early stopping criterion for iterative LDPC decoder, saving a considerable amount of energy.
- Configurable amount of LDPC decoding iterations for trading-off throughput and error correction performance.
- Collection of statistic information (number of iterations, decoding success).

CCSDS LDPC Encoder

Key benefits of the encoder are:

- High-throughput, low-latency encoder core.
- Low-power and low-complexity design.
- No BRAM required.

Performance Figures

- 1.6 Gbit/s coded throughput at 200 MHz
- Decoding latency of 4.3 μs at 5 layered decoder iterations and 200 MHz
- Encoding latency of 40 ns at 200 MHz

Features

- Support for code rate 223/255 (7136/8160)
- Coded block size 8160 bits
- Compliant with “TM Synchronization and Channel Coding, Recommended Standard, CCSDS 131.0-B-3, Blue Book, September 2017”.

Applications

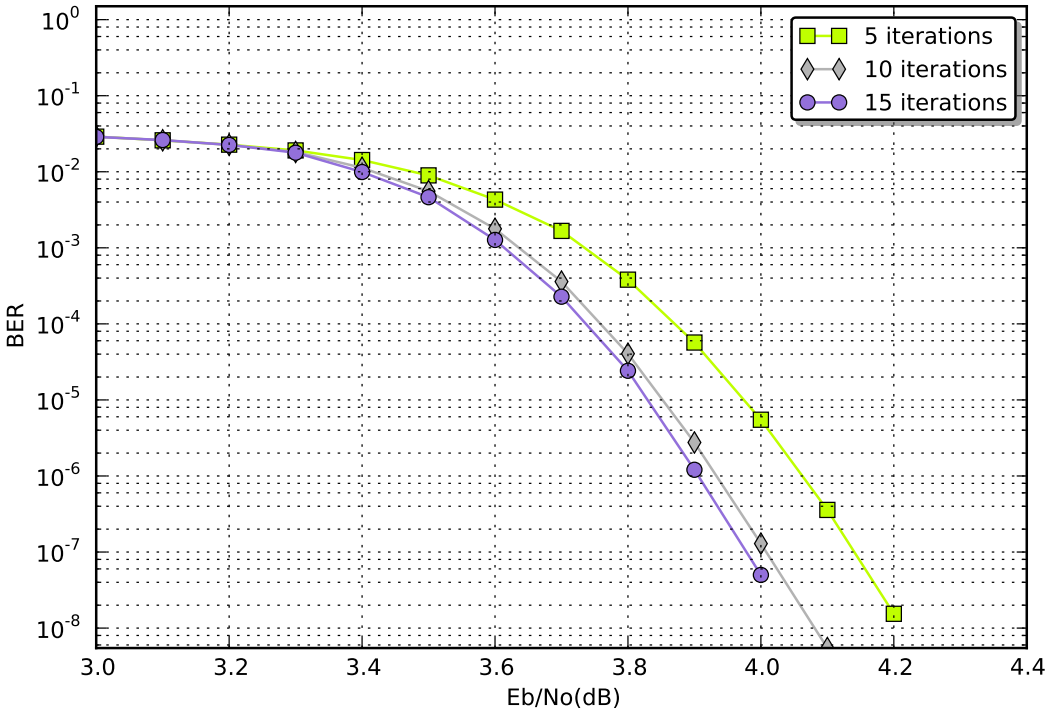
- Near-Earth and Deep-Space communication.
- Space links communication.
- Space internetworking services.
- Microwave Links
- Optical Links
- Further High-throughput Applications

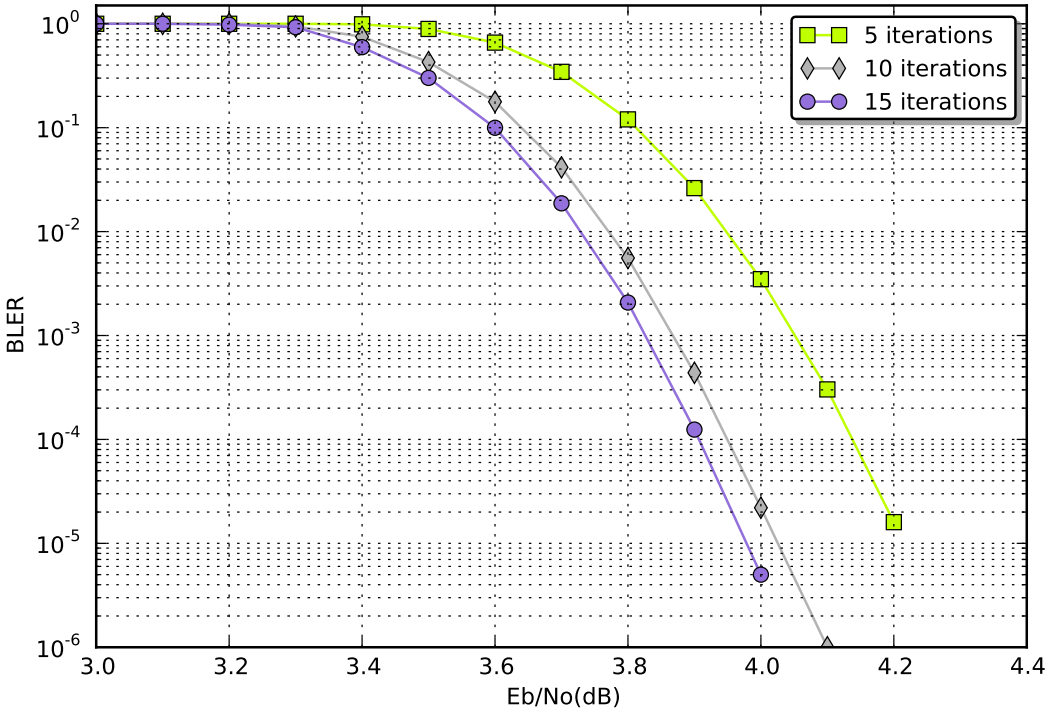
Deliverables

- VHDL source code or synthesized netlist
- HDL simulation models e.g. for Aldec’s Riviera-PRO
- VHDL testbench
- bit-accurate Matlab, C or C++ simulation model
- comprehensive documentation

Error Correction Performance

The following figure depicts bit error rate (BER) and block error rate of the CCSDS LDPC decoder.





Related Products

CCSDS SCCC Turbo Encoder and Decoder

CCSDS AR4JA LDPC Encoder and Decoder

DVB-S2X LDPC/BCH Decoder

DVB-RCS2 Turbo Decoder

About Creonic

Creonic is an ISO 9001:2015 certified provider of ready-for-use IP cores for wired, wireless, fiber, and free-space optical communications. All relevant digital signal processing algorithms are covered, including, but not limited to, forward error correction, modulation, equalization, and demodulation. The company offers the richest product portfolio in this field, covering standards like 3GPP 5G, DVB-S2X, DVB-RCS2, CCSDS, and WiFi. The products are applicable for ASIC and FPGA technologies and comply with the highest requirements with respect to quality and performance. For more information please visit our website at www.creonic.com.

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