

## **Product Highlights**

- High-performance, easy-to-use core
- PCI Express™ Base Specification Revision 3.0/2.0/1.1 compliant
- x1, x2, x4, x8, x16 lane support
- 8.0, 5.0 & 2.5 Gbit/s SERDES support
- 1-8 Physical Function support
- SR-IOV support with up to 255 Virtual Functions
- Endpoint, Root Port, Upstream Switch Port, Downstream Switch Port, Bifurcation support
- 32, 64, 128 and 256 bit Core width support
- Transaction Layer Bypass option
- AER, ECRC, MSI-X, Multi-Vector MSI, Lane Reversal support
- Delivered fully integrated and verified with target PCIe PHY
- Provided with a PCI Express Testbench
- Fully validated
- · Minimal ASIC gate count
- Source code available
- Customization and Integration services available

## **Block Diagram** Expresso Core or x8 PHY TX DATA TX PHY TX TRANS TX Serial TX VC0\_TX LINK Express x1, x2, x4, LAYER LAYER LAYER Local Interface INTERFACE PHY (Internal External) PHY RX Serial RX VC0\_RX DATA 짇 PHY TRANS LINK LAYER LAYER **LAYER** Status Error Info MGMT CLK CONFIGURATION AND MANAGEMENT CFG\_EXP CONFIGURATION REGISTERS

## **Product Overview**

The Expresso 3.0 Core is part of Northwest Logic's PCI Express Solution. This solution is designed to achieve maximum PCI Express throughput while being easy to use.

The Expresso 3.0 Core separately, or in combination with Northwest Logic DMA Core and DMA Driver, provide the maximum system throughput on a PCI Express link. Contact Northwest Logic more details.

The core is specifically designed for ease of use including full receive packet decoding, complete error handling, automatic handling of PCI Express message packets and comprehensive system-debug and link monitoring support.

The core is delivered fully integrated and verified with the user's Target PHY. Contact Northwest Logic for a complete list of supported PHYs. To accelerate simulations, the core is also delivered integrated with a fast simulating behavioral PHY.

The core is also provided with the Expresso Testbench which provides a PCI Express Bus Functional Model.

The core is fully compliant with the current version of the PCI Express Base Specification 3.0. The core includes all of the required 3.0 features including Physical functions, SR-IOV, flexible equalization support. To keep clock rates manageable, Northwest Logic also supplies a 256 bit side version of the core.

The core has been extensively validated with the Avery Logic PCI-Xactor PCI Express Compliance Suite and Northwest Logic Expresso Testbench.

Northwest Logic also provides IP Core customization services. Contact Northwest Logic for a quote.

## **Product Deliverables:**

- Core (Netlist or Source Code)
- Testbench (Source Code) with support for Aldec
- Complete Documentation
- Expert Technical Support & Maintenance Updates