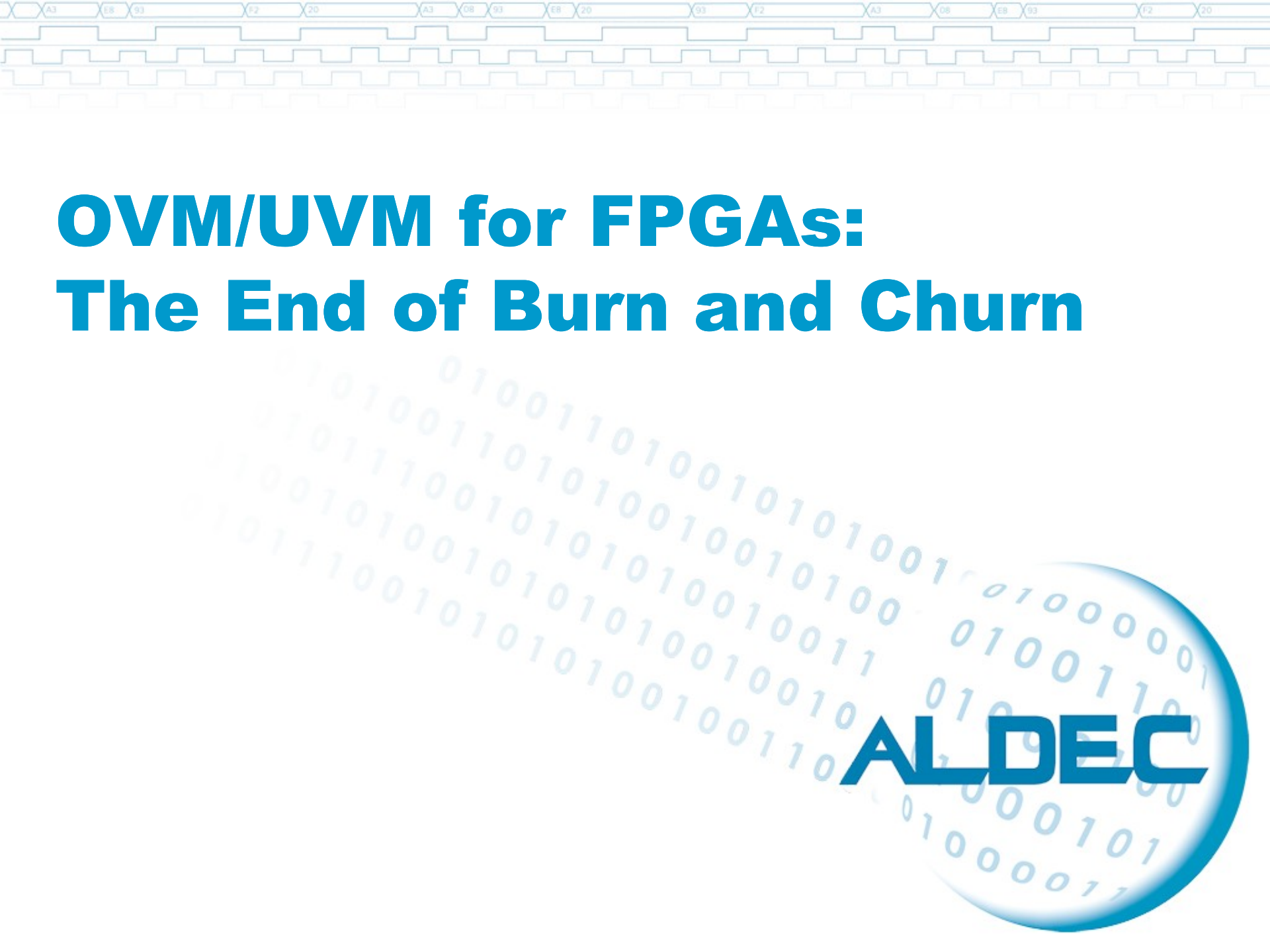
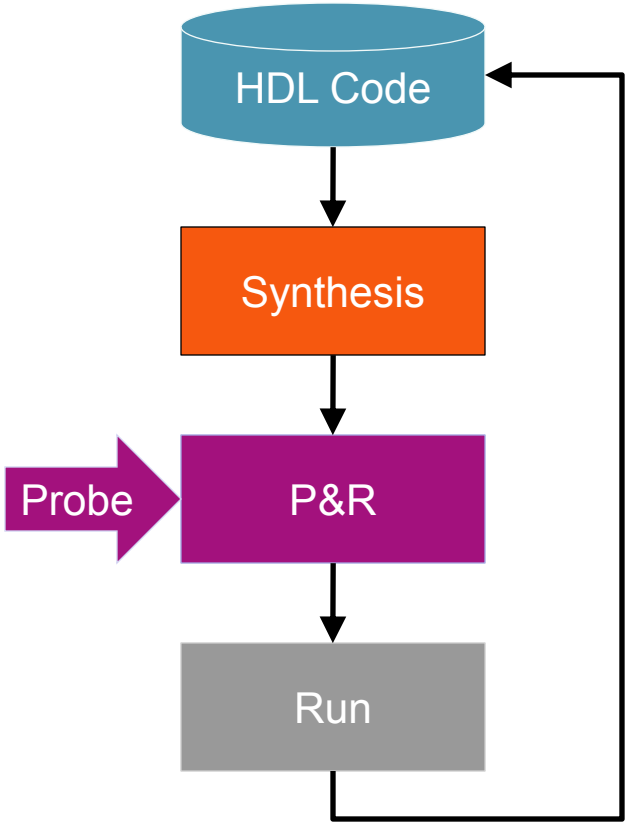
OVM/UVM for FPGAs: The End of Burn and Churn



FPGA Verification by In-Circuit Test

"Burn and churn" based on at-speed test with real input

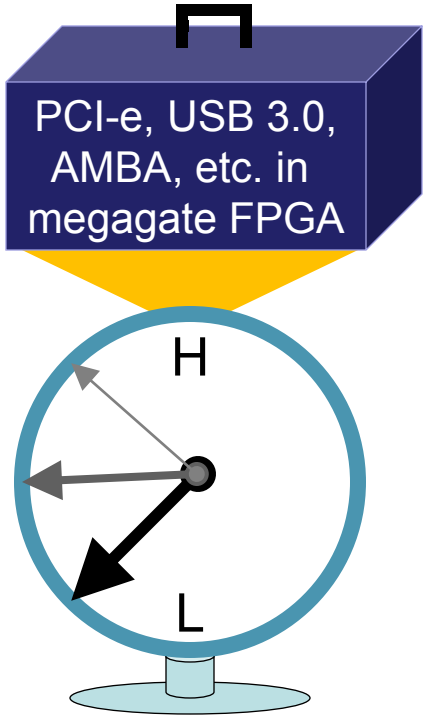
- Shortest path to the lab
  - Nominal simulation of RTL blocks
  - Relatively short synthesis/ P&R cycle with at-speed run
- Real-world verification
  - Stimulus from bench testers or actual in-circuit input
- Probes provide observability
  - Critical nodes retain during programming
  - Debug and respin



Design Requirements Pressure Methodology

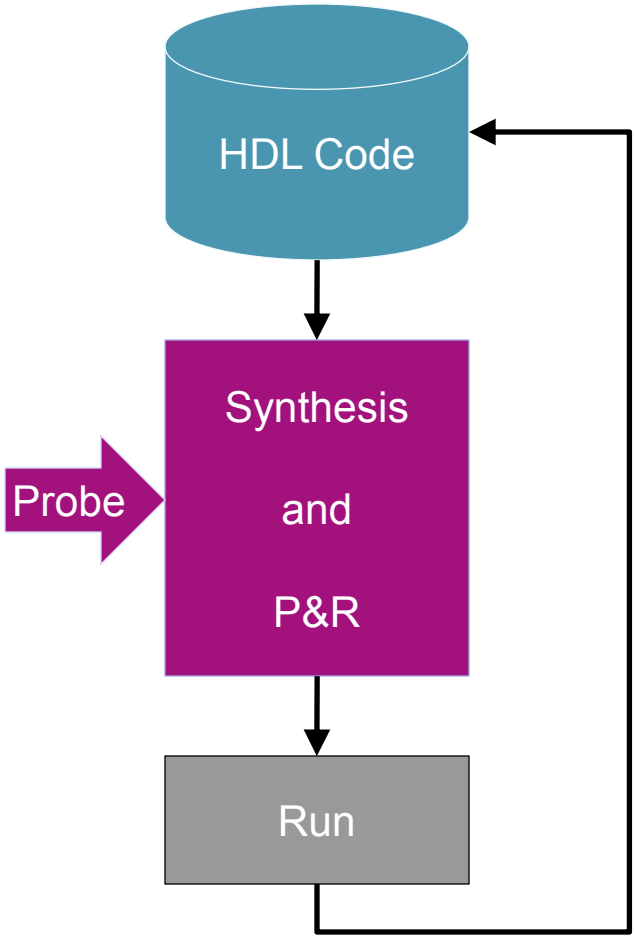
Bigger designs and more standard protocol use

- Mega-gate FPGAs depend on IP
  - Block-level verification by the vendor
  - Deep hierarchy reduces engineer's ability to know the whole design
- State-space grows exponentially
  - Increasingly difficult to create corner cases in the lab with only directed testing
- Must verify protocol interaction
  - Assuming each protocol is verified, how do they interact in the system?



Weighing Down Observability and Controllability

Predictability of Burn and Churn is Gone

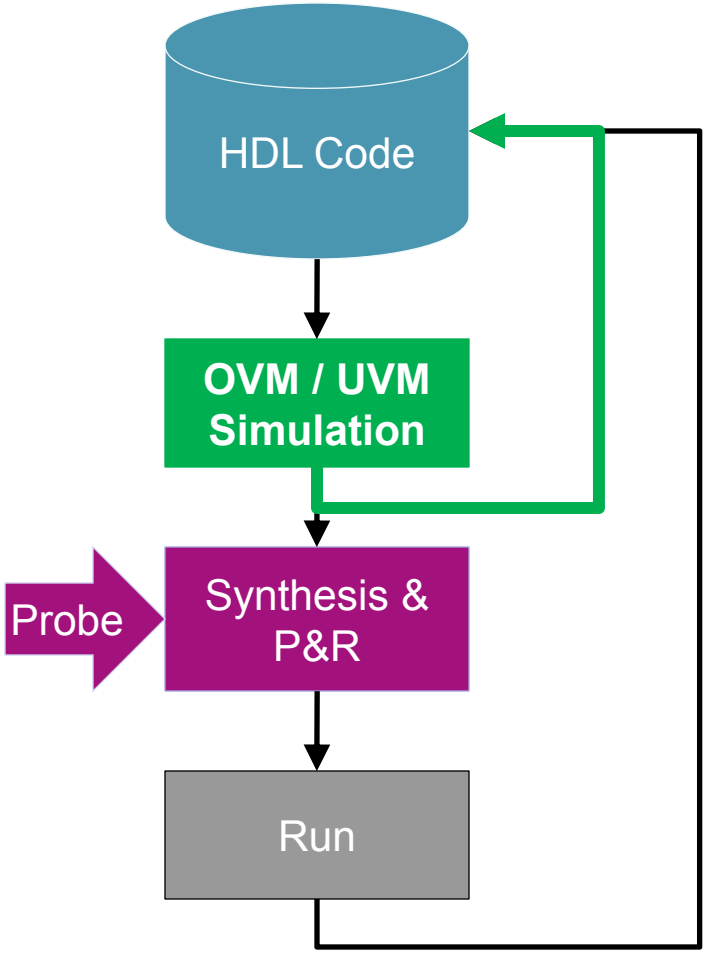


- "Burn" is now the long-pole
  - Synthesis and P&R merging due to FPGA complexity
  - "Burn" time is approaching system simulation speed
- "Run" is fast but unobservable
  - Changing probes forces new programming
  - Design too large to "know"
  - Difficult corner case testing
  - Debug becoming incremental – where is the end?

OVM/UVM Increases FPGA Verification Quality

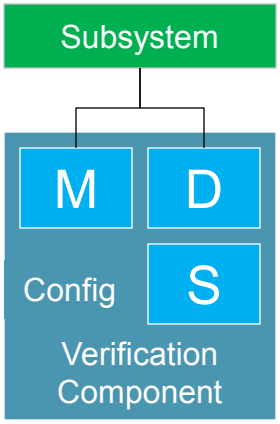
Observability and controllability augment in-circuit

- Fully observable simulation
  - Assertions heighten observability with temporal monitoring key to complex protocols
  - Coverage measures verification progress against plan
- OVM / UVM augments in-circuit
  - Scalability via verification components from block to system
  - Controllability via virtual sequences
  - Reuse via factory localization

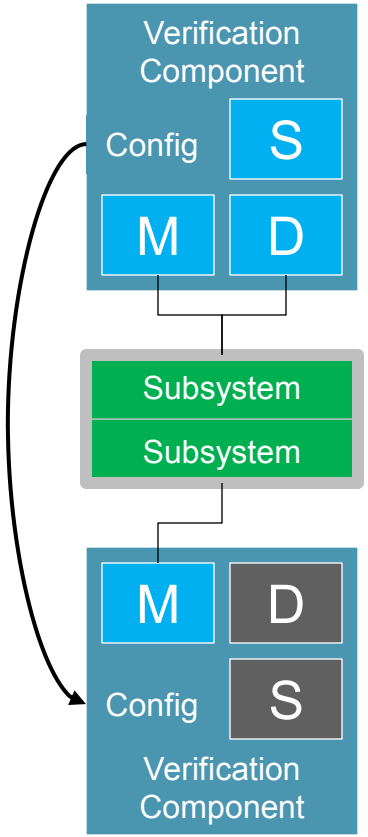


FPGA SoC is All About Rapid Assembly

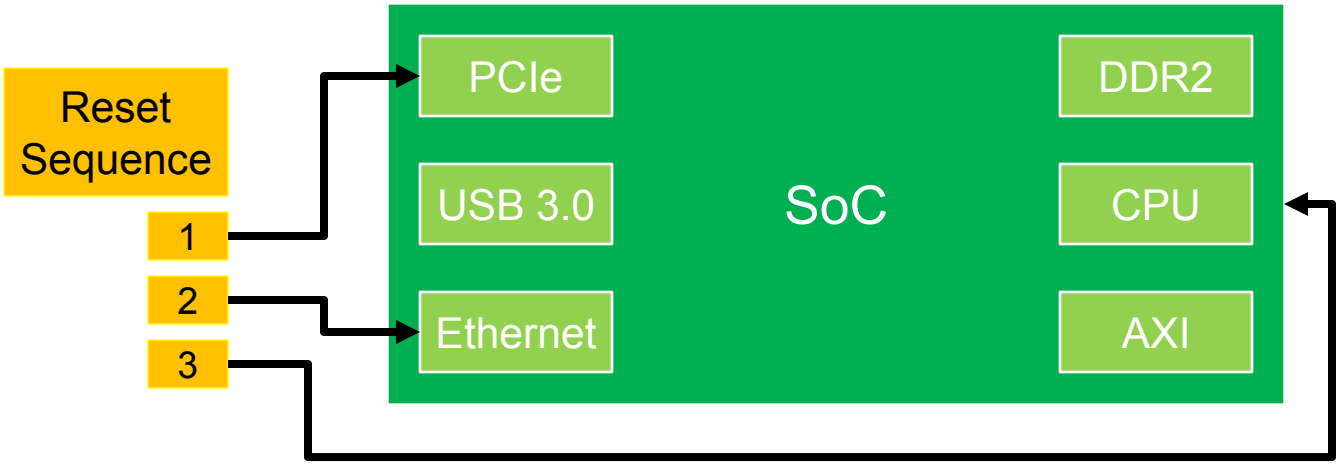
OVM/UVM verification components scale with SoC



- Verification component
  - Driver, monitor, sequencer separated for modular implementation
  - Configuration lives within the component
  - Consistent TLM channel for component connection
- Rapid verification environment assembly
  - Components configure hierarchically
  - Lower-level components switch to passive
- *Reduces burn-and-churn test reconfiguration effort*



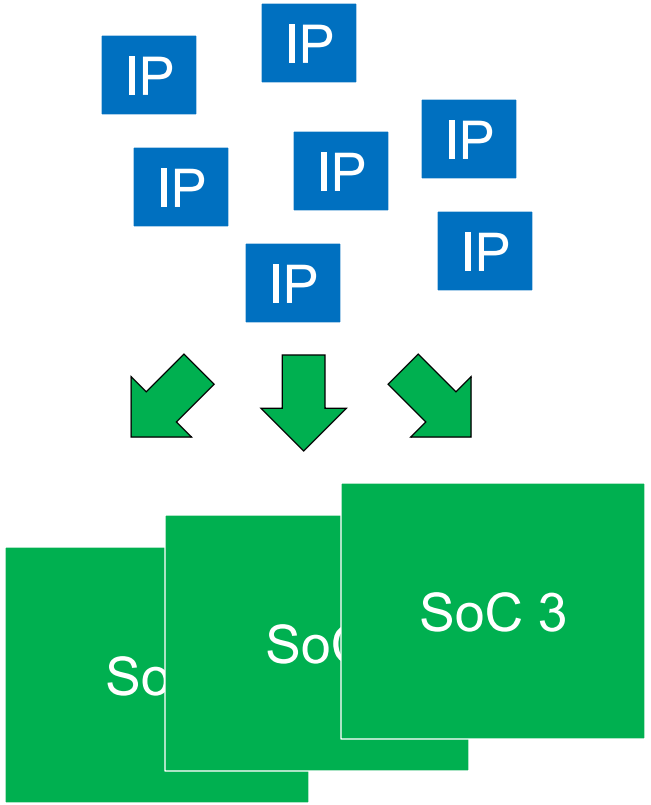
Virtual Sequences Reach Corner Cases



- Reset sequences unique to an SoC configuration
  - Virtual sequences enable rapid debug of reset
- Creating and randomizing difficult real world conditions
  - Coordinated events on multiple interfaces
  - Asynchronous activity on multiple interfaces (pushing to the limit)
- *Reduces lab time set up; going beyond limited directed tests; exhaustive testing*

Reuse, Reuse, Reuse

- FPGA engineers pull IP from many suppliers
  - OVM/UVM assures consistent verification IP for rapid integration
  - Today's top-level IP may be deeply embedded tomorrow as FPGAs grow
- FPGA architecture lends itself to rapid derivative creation
  - OVM/UVM factory enables localization without changing code
- OVM/UVM improves productivity in derivative creation and supplier interaction



FPGA Engineers: Escape Burn-and-Churn!

Learn and apply OVM/UVM

- Burn-and-churn is on the run
  - Driven by lack of observability and controllability in in-circuit FPGA testing
  - At-speed (in-circuit) tests will still be part of FPGA verification
- OVM/UVM simulation available for all FPGA engineers
  - Not just for high-end FPGA/ASIC anymore
- Multiple resources for OVM/UVM
  - OVMWorld.org and UVMWorld.org
  - Multiple training resources available
- Aldec's Riviera-PRO simulator supports
  - OVM 2.1.1
  - UVM-EA release