Lab 4 -Compilation and Simulation

In the previous three lab session you have created a HDL model of an eight bit Grey Counter (GCounter(RTL)), a top level block diagram (top(top)), and a Controller finite state machine (Controller(Controller)), each of these have been compiled and the results are shown in the **Design Browser - Files** Tab Figure 69. Currently the files are shown in the order they were created, however this currently means that the top-level block diagram is compiled before the controller FSM it uses, this will cause a compilation warning.

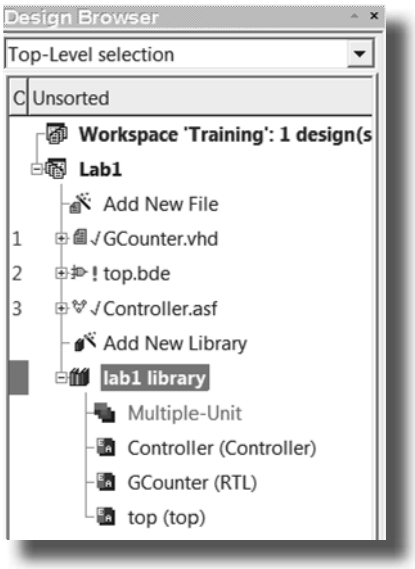

Figure 69: Design Browser after File Creation

To resolve the issue you could delete the simulation data in the library and then do a recompile with file re-order ( or **Design→Compile All with File Reorder**), or manually change the file order.

70. To manually re-order the files, left-click the top.bde symbol  in the design browser and drag it below the Controller.asf  icon. The location that the file is going to be place is indicated by a line between the files in the **Design Browser**. Once in position drop the file Figure 70.

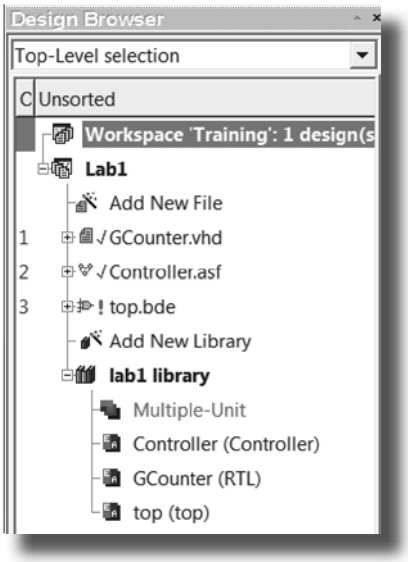

Figure 70: Reordered Design Browser - Files Tab

As you can see from Figure 70, the design library lab1 has compiled units from your earlier compalations, sometimes you may wish to remove all the compiled design entities from