

FPGA Design & Verification in Aldec Active-HDL

Lab 3 – FSM Editor

The final step for finishing this simple design is to describe the controller block added in the last Lab.

51. Double Left-Click the controller block in the top Block Diagram, normally this would descend a hierarchical block, but because the underlying block has not been described the **Create New Implementation** dialogue will be launched, so that

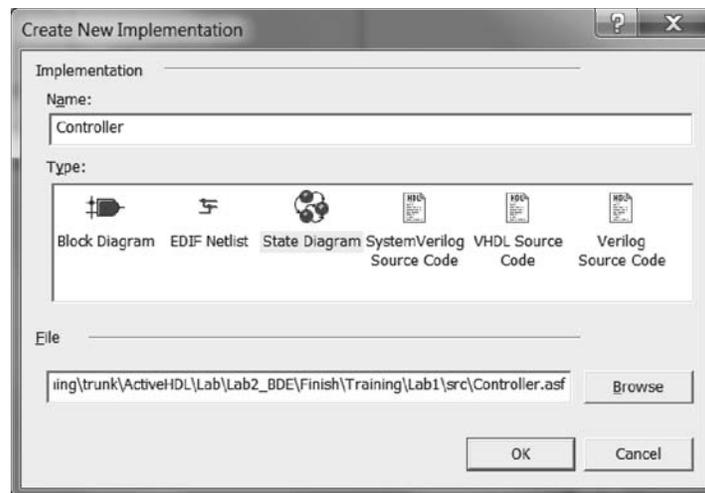


Figure 46: Create New Implementation Dialogue

the underlying structure can be defined.

52. In the dialogue select State Diagram, note that the File details will be automatically filled in based on the file type selected and the name of the calling FUB.
53. Click **OK**.
A new Finite State machine diagram will be added to the Design Browser and the FSM will be opened, Figure 47.