

## FPGA Design & Verification in Aldec Active-HDL

### Lab 2 – Block Diagram Entry

31. Double click the **Add New File** icon in the design browser to launch the Add New File dialogue

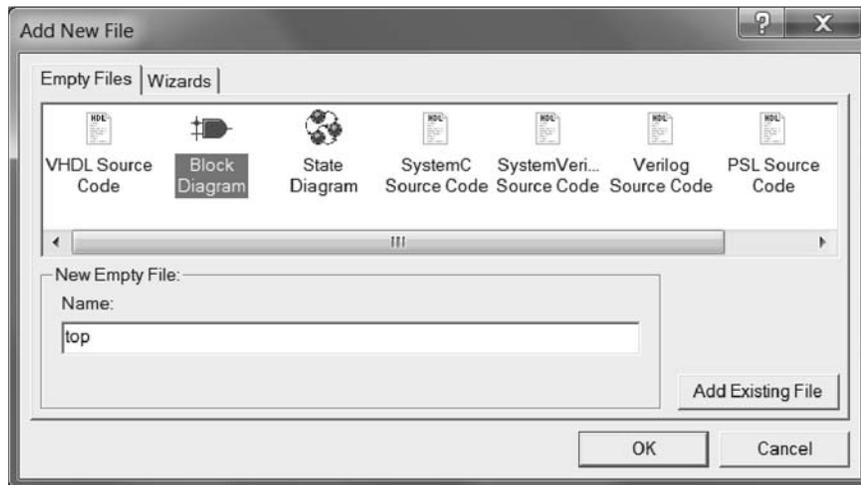


Figure 24: Add New File – Block Diagram

32. Select **Block Diagram** and set the **New Empty File; Name:** to `top`, (See Figure 24) and click **OK**.

A new empty block diagram called `top.bde` will open as shown in Figure 25, with the block diagram editor open you can start your design by adding:

- Symbols
- FUBs
- Processes
- Terminals

33. Click the Show Symbols Toolbox icon  or select **View→Symbol Toolbox** from the drop down menu or use the **S** hot key, to open the Symbol toolbox, which will open by default to the right of the Block Diagram Canvas. The toolbox is shown in Figure 26

The Symbol tool box is split into two sections the