Fast Track
Training Series from ALDEC

Fast Track to UVM

3-Day Training Seminar

Who Should Attend:
Hardware Design Engineers
Verification Engineers
Quality Assurance Engineers/Mgrs
Project/Program Managers

Fast Track To UVM

3-Day Training Seminar

Course Overview:
3-day intensive Universal Verification Methodology (UVM) training, created for HDL designers with solid working knowledge of SystemVerilog design.

This training provides attendees the solid background and practical experience required to create their first UVM test environments. Items such as transactions, sequences, drivers, sequencers, monitors, agents, tests, etc. are explained in detail. Advanced concepts are also introduced to facilitate further education, along with hands-on exercises.

DAY 1
UVM Background
UVM High-Level Overview

DAY 2
Managing UVM Verification Environment
Building Verification Components

DAY 3
Using UVM
Advanced Features Overview

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THE DESIGN VERIFICATION COMPANY

Seating is limited.
Register today at www.aldec.com/events.

$1995 3-day course registration.
For more info, please call **702.990.4400** or email **training@aldec.com**.

2012 Schedule

Dallas, TX *Sept 18-20*
Irvine, CA *Oct 2-4*
Tempe, AZ *Oct 16-18*

3-Day '**Fast Track to UVM**' Training Seminar

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DAY 1 AGENDA

UVM Background:

- Object Oriented Programming
- Transaction-Level Modeling
- Constrained Random Stimulus
- Functional Coverage

High-Level UVM Overview:

- High-Level UVM Overview
- Verification Components
- Data Items
- Environments, Tests and Top Level
- UVM Classes
- Factory
- Phases

DAY 2 AGENDA

Managing UVM Verification Environment:

- Navigating UVM class hierarchy
- Factory and Configuration Database

Building Verification Components:

- Data Items and Sequencers
- Connecting TLM Components with DUT (Virtual Interfaces)
- Drivers, Monitors, Agents, etc.
- Instantiating and Connecting Components
- Creating Environments and Tests
- Tying Loose Ends: Top-Level Module

DAY 3 AGENDA

Using UVM:

- Building Test Class
- Virtual Sequences
- Scoreboards
- Implementing Coverage Model

Advanced Features Overview:

- Register Layer
- Using Factory
- Callbacks
- Sequence Library
- Command Line Control

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About Trainer: Jerry Kaczynski, Aldec Research Engineer
Jerry possesses 20+ years experience in HDL language & tool training, technical writing, application and research engineering. He is an IEEE and Accellera committee member, involved in the development of industry standards for VHDL, Verilog, PSL, SystemC & SystemVerilog.

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