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Design Entry & Management

Creating HDL Text Modules

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v2.1

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Bottom-Up Design

- Start by creating a new workspace and design
  - Use the **New Source File** Wizards
  - Add existing files
  - Create an empty design
- Complete the source code
- Check syntax for errors
- Verify the functionality of the design
- Create a top-level diagram or entity

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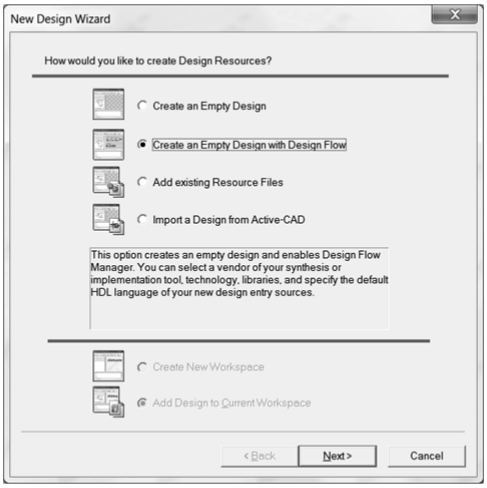
Note:

Verification is an important step in the design process, verification at the HDL level allows for testing of scenarios that may be very difficult to test for in the physical hardware. With small designs, it is possible to verify their correct function using simple simulations and visual checks of the output waveforms, however modern complex design containing 1000's if not 100,000's of lines of code need comprehensive verification, using approaches such as assertions, code coverage and design rule checking. Verification methodologies, assertions, code coverage and design rule checking are beyond the scope of this course, however Aldec have training available on these subjects.

Whatever design flow you are using be it top down, bottom up or a mix of the two the methodology is the same, the first step is always to create a new workspace and design. Active-HDL uses the concepts of workspaces and designs, a workspace can be thought of as a project and can hold one or more designs, and each design will have one or more libraries, for compiled HDL code. Active-HDL by default will maintain a fixed workspace hierarchy on the computer file system, however this may not fit with your company design standards, if this is the case that you can enable flexible file management, this allows you to store files as you require;.

Once the design is created then you need to add the source HDL for the design, be that HDL code written using Active-HDL's code editor, or be it derived from graphical representations, such as block or finite state machine diagrams, you can also add IP from other designs or third parties. This code need to be compiled which will check for syntax errors and then the design needs to be functionally verified.

The Design Wizards



The **Design Wizard** simplifies the process of creating your initial workspace and design, Active-HDL makes extensive use of wizards that guide you through the initial stages of a design development.

For any design the first thing to do is create a new workspace **(File→New Workspace)**. And specify its name; you can also selecting **Create New Workspace** from the start-up dialogue, immediately after launching Active-HDL.

In the **New Design Wizard** window four selections can be made:

- To create an empty design, check the Create an empty design option.
- To create an empty design with design flow, check the Create an empty design with design flow option, enabling the design flow option allow you to setup the synthesis and P&R tools you wish to use with your design, and control them all from within the Active-HDL environment.
- To add existing files, check the Add existing resource files option. Select the source files in the Open window and finish the design creation by clicking the Finish button.

Note:

To set up a new design, it's also possible to select the Design option in the File→New menu.

The attached resource files could be:

- VHDL Source Code (vhd, vhdl, vhq, tvhd, vho, vhm, vhi)
- Verilog Source Code (v, vei, veo, vo, vm, vmd, vlb, vlg)
- C/C++ Source Code (c, cc, cpp, cxx, h, hh, hpp, hxx)
- C/C++ Configuration (.dlm)
- Verilog Value Change Dump (.vcd)

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