Object View

		VCC0 MICROCONTRO	DLLER 8051	Design Unit Header Ibrary IEEE: use WEREKINSER all: use WUREKINSER all:	01-01-0				Î			6
		<u>uo</u>		use monorganism,	B4 Generics	Terminals (omponer	ts Signals Instances	Processes	Signal	assignments	• 7
	CLKID	Ci. K		PORT0(7.0)	A1 Name	1	Direction		Initial	Value	Hidden	-
	RESETID-	467 P40(70)	PORT1(7.0)	T	CLK		h	STD LOGIC	mou	V GIGG	No	
		- P10/70	PORT3(7-0)		KEY 0		In	STD LOGIC			No	- 1
		110074			KEY 1		In	STD LOGIC			No	
		AL8001		FPGA DEVICE	KEY 2		In	STD LOGIC			No	
				U1	KEY 3		In	STD LOGIC			No	=
				PORTIG 0) PORTIG 1)	KEY 4		In	STD LOGIC			No	
		l r	Fub Properties	127.0	KEY 5		In	STD LOGIC			No	
			e de la companya de l		KEY 6		In	STD LOGIC			No	
			General Pin List Por	rwapping Generics Attributes View Texts	KEY_7		In	STD LOGIC			No	- U
			Name	Mapping Ty Function/Value	KEY 8		In	STD LOGIC			No	
			PORT0(70) · In mod PORT0(70) · Out mod	e Default Default	KEY 9		In	STD LOGIC			No	
		KEYBOARD CONTI	PORT1(3.0)	Default	oWBS		In	STD LOGIC			No	-
		LOOIC	PORT2(7.0)	Default	1							
	L		RESET	Default					_	_		
	KEY_00	(i)_1	CODE(3.0)	Default	1		PINS OF PAR	ALLEL - SERIAL REGISTER TO SERIAL PORT OF 8051				_
	KEY_2D		ADDRESS(4:0)	Default				D BUSY	•			
	KEY_30- KEY_40-	(4)_1 (40063.0)	nCS	Default				2000 C	•			
•	KEY SID-		CTR	Default				CIDATAS(7:0)				
-			nRD nWB	Default								
			ACKA	Default						_		
			BUSY	Default								
			DATAS(7:0)	Default								
					Details							
						1						

The Objects View dock-able window can be opened using

View→Objects or by clicking , the object view allows you to view, sort and change properties of all objects defined in a block diagram e.g. terminals, signals, generics, parameters, statements.

The objects listed within this window can be put in a user-defined order by using drag and drop.

They can also be sorted in ascending or descending order or with the default settings.

The final order applied by the user is used while generating HDL code. Additionally, the **Objects View** window allows the user to follow signals/net and processes specified on block diagrams.

Multiple Architecture Support

Multiple Architectures Support



The Block Diagram Editor allows the user to generate VHDL code that contains an architecture body only.

In this way different implementations (several architectures) for the same entity can be created and used, this is very useful in the early design stages were there may be a certain amount of 'What If' analysis being made, before committing to a defined architecture for

Code Generation Set	tings ? X						
Design Unit Gener	ation Conversion Functions Packages List Libraries						
Design Unit:	top						
<u>A</u> rchitecture:	top						
Design Unit Head	Generate Architecture Only						
library IEEE: use IEEE.std_logi use IEEE.std_logi use IEEE.std_logi use IEEE.std_logi	y IEEE; EEE.std_logic_1164.all; EEE.std_logic_arith.all; EEE.std_logic_signed.all; EEE.std_logic_unsigned.all;						
	OK Cancel						

Figure 16: BDE Code Generation Settings

the design.

Access the required code generations settings from the menu using **Diagram→Code Generation Settings Design Unit** Tab and check the **Generate Architecture Only** check box.

It is also possible to access the **Design Unit Header** information from the **Design Unit** tab of the **Code Generation Settings**, this allows the setting of the library and use statements when using the BDE to generate VHDL code.

Visible Port Directions

Visible P	Port Direction	
Preferences Category:	Block Diagram Editor	
Advanced options Performance Optimization Compliation B: VHDL Compiler	General : Crosshair cursor visible Pins direction visible Rulers visible Visible Visible Visible Auto scrolling	U1
(E) Verilog Compiler Linting – ALINT Simulation – Assertions – Debugger – Assertions	Default instance name prefix: U Unit inch Right-click action: Draw fub	→ Pin1 Pin3 ↔
- Memory Management - Advanced Dataflow - Riviera-PRO Generation - Viell Case	Autorouting	- Pin2 Pin4 🖝
Verilog Standard ⊞ Verilog Standard ⊕ Tiel Headers ⊕ Copy Instantation Editors ⊕ HoL Editor ⊕ 10054 Borgram Editor ⊕ State Diagram Editor ⊕	Grid visible Snap to grid Grid 0.100 inch	WHC
Setup	Default OK Cancel Apply	
v2.1	FPGA Design & Verification in Aldec Active-HDL	THE DESIGN VERIFICATION COMPA

The purpose of this feature is to make the port direction visible on a block diagram.

This makes the analysis of a block diagram easier especially when it contains a large number of complex symbols that have different types of ports located on the left and right side of the symbol. This option is accessed from the **Tools→Preferences→Editors→Block Diagram Editor**