

Advanced Verification Platform



Riviera-PRO™

Riviera-PRO verification platform delivers advanced design entry, simulation, debugging, and verification tools based on cutting edge technology. Riviera-PRO integrates an extensive set of tools and features that delivers efficient FPGA and ASIC design and verification.

Top Features

- Advanced Verification Platform (UVM/OVM, VMM)
- Different Levels of Abstraction (ESL/TLM, RTL, Gate-Level)
- High-Performance Simulator for Mixed Language Designs
- IEEE VHDL, Verilog®, SystemVerilog, SystemC/C/C++
- Transaction-Level Debugging Environment
- Assertion-Based Verification (SVA, PSL and OVA)
- Code and Functional Coverage
- DSP Co-Simulation with MATLAB® and Simulink®
- Linux and Windows® 7/Vista/XP/2003 32/64 Bit Support

Advanced Verification

Riviera-PRO includes advanced verification toolset for functional verification of complex FPGA and ASIC designs. The platform supports the latest version of Universal Verification Methodology (UVM) and enables building up layered, coverage driven, transaction-level verification environments that can be reused across different designs and different platforms. The Assertion-Based Verification (ABV) is available based on SystemVerilog and Property Specification Language (PSL) and enables deploying coverage driven methodology.



High-Performance Simulator

Riviera-PRO incorporates industry-leading simulation optimization algorithms to achieve the highest performance in mixed-language simulation at various levels of abstraction (transaction, register transfer, and gate level).

Integrated Debugging Environment

Riviera-PRO's integrated debugging environment supports all standard languages and provides intuitive ways to visualize and analyze key objects in your design. Integrated debugging tools provide code tracing, waveform, dataflow, coverage, and memory visualization capabilities. Native support of the TCL language provides the means for configuring and controlling graphical and simulation parameters with the use of the script files.



STANDARDS



SILICON



INTERFACES



FEATURES

PRODUCT CONFIGURATIONS

	LV	LVT	LVT-SV
Supported Languages			
VHDL IEEE 1076 (1987, 1993, 2002 and 2008)	•	•	•
Verilog® HDL IEEE 1364 (1995, 2001 and 2005)	•	•	•
SystemVerilog IEEE 1800™-2005 (Design)	•	•	•
SystemC™ 2.2 IEEE 1666™/OSCI 2.2/TLM 2.0	Option	•	•
SystemVerilog IEEE 1800™-2005 (Verification)			•
Design Entry and Design Management			
HDL Editor with Syntax highlighting and Auto-Complete	•	•	•
File Browser, Design and Library Managers	•	•	•
Customizable GUI Perspectives	•	•	•
Macro, Tcl/Tk, Perl script support	•	•	•
HDL Debug and Analysis			
Interactive Code Execution Tracing	•	•	•
Advanced Breakpoint Management	•	•	•
Accelerated Waveform Viewer (ASDB)	•	•	•
Hierarchical References to/from VHDL (Signal Agent)	•	•	•
Post-Simulation Debug	•	•	•
Waveform Compare	•	•	•
Assertions in Waveform and Debugging	Option	•	•
Memory Viewer	•	•	•
Integrated C/SystemC Debugger		•	•
X-Trace	Option	•	•
Advanced Dataflow	Option	•	•
Simulation/Verification			
Single or Mixed Language	•	•	•
Verilog Programming Language Interfaces (PLI/VPI)	•	•	•
VHDL Programming Language Interface (VHPI)	•	•	•
SystemVerilog IEEE 1800™-2005 DPI 2.0	•	•	•
Value Change Dump (VCD and Extended VCD) Support	•	•	•
Incremental Compilation	•	•	•
Multi-Threaded Compilation	•	•	•
32/64-Bit Cross-Compatible Libraries	•	•	•
Simulation Model Protection/Library Encryption	•	•	•
VHDL 2008 and Verilog 2005 IEEE Encryption	•	•	•
Xilinx® SecureIP Support	Option	•	•
Language-Neutral Altera® Libraries	Option	•	•
Verilog and VHDL Performance Optimization		•	•
64-bit Simulation		•	•
Transaction-Level Visual Debugging		Option	•
Profiler (Performance Metrics)	Option	•	•
SFM (Server Farm Manager)	Option	Option	•
HES™ Hardware Assisted Verification (Acceleration and Emulation)	Option	Option	Option
OVM and UVM Support			•
Assertions and Coverage			
PSL IEEE 1850, SystemVerilog IEEE 1800™, OpenVera Assertions	Option	•	•
Code & Toggle Coverage and UCIS-compatible Database	Option	•	•
Functional Coverage			•
External Simulation Interfaces			
Synopsys® SmartModels, SWIFT Interface and LMTV	Option	•	•
SpringSoft® Verdi™ PSD mode Interface	Option	•	•
Co-simulation			
Simulink® Co-simulation	•	•	•
MATLAB® Co-simulation	Option	•	•
Design Rule Checking			
ALINT™ with Aldec Basic Rule Library	Option	•	•
DO-254 VHDL or Verilog Rule Library	Option	Option	Option
STARC® VHDL or Verilog Rule Library	Option	Option	Option
Reuse Methodology Manual (RMM) Rule Library	Option	Option	Option
Supported Platforms			
Windows® 7/Vista/XP/2003 32/64 bit	•	•	•
Linux 32/64 bit	x86 Only	•	•



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