HES-7™ | ASIC Prototyping

Scalable, Flexible Solution

HES-7™ provides SoC/ASIC hardware verification and software validation teams with a high quality FPGA-based prototyping system, scalable up to 633 million ASIC gates. HES-7 is ideal for ASIC prototyping, complete SoC integration or sub-system validation The HES-7 platform utilizes Xilinx® Virtex®7 or Xilinx UltraScale® FPGA-based boards. Each HES7XV4000BP board contains two Xilinx Virtex-7 2000T and has up to 24M ASIC gates of capacity, while the HES7XV12000BP board contains six Xilinx Virtex-7 2000T and delivers up to 72M ASIC gates, and the latest HES-7 HES7US2640BP board contains six Xilinx UltraScale-440 FPGAs providing up to 158M ASIC gates capacity per board. The HES-7 prototyping solution was architected to provide easy implementation and expansion in a rack form factor with a non-proprietary backplane for flexible, scalable hardware configurations.

Top Benefits

- **Available in a scalable capacity up to 633 million ASIC gates**
- **Up to six FPGA on a single board and scaled to twenty four on the backplane configuration**
- **Non-Proprietary daughter board connectors for external peripherals and interfaces**
- **Peripherals and interfaces via daughter cards including ARM® Cortex™ support with Xilinx Zynq™**
- **Supports sub-systems prototyping and complete SoC integration**
- **Prototyping hardware reuse for acceleration and emulation verification modes**
- **Fast USB based utility for FPGA programming and board configuration**
- **Rack form factor chassis for backplane configurations**
- **Superior quality backed by industry leading 1-year warranty**
- **Trusted EDA vendor with over 30 years of experience in verification and FPGA prototyping**

SoC Extension Daughter Board with ARM®

The HES-7™ platform capabilities are extended with the unique SoC Daughter Board featuring out-of-the-box support for the dual-core ARM® Cortex®-A9 with Xilinx Zynq-7000 SoC FPGA that enables quick prototyping even without the availability of ARM RTL code. The speed-optimized ARM Cortex, running a Linux operating system, Android, or FreeRTOS, connects to the rest of the SoC blocks in HES-7 via a standard AMBA AXI/AHB bus. Additionally, the SoC daughter board provides a variety of peripherals for the most common SoC interfaces:

- Networking & Wireless: Gb Ethernet, WLAN 802.11 b/g/n and Bluetooth® v2.1
- Multimedia: HDMI and Audio codec
- I/O : USB, 2.0/OTG, SPI/I2C, RS232 and GPIO
- Storage: SD Card and SPI/I2C/NAND Flash

HES-7™ Boards	Backplanes	Daughter Boards and GPIO Extenders
• HES7XV4000BP (2x V7-2000, up to 24MG) • HES7XV12000BP (6x V7-2000, up to 72MG) • HES7-UltraScale (6x UltraScale-440, up to 158MG)	• BPx4 (4x HES-7 slots) ◦ HES7XV4000BP: up to 96MG ◦ HES7XV12000BP: up to 288MG ◦ HES7-UltraScale: up to 633MG (Q3/Q4 2015) • BPx4_DBx2 (4x HES-7 slots + 2x DB slots)	• SoC Daughter Board (Zynq/Cortex-A9, Ethernet, Multimedia, Memories) • HES-7DB_CONNECT3 (Ethernet, Flash Memories, PCIex8, GPIOs) • HES-7DB_CONNECT4 (Molex to Samtec bridge)

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THE DESIGN VERIFICATION COMPANY

	HES7-4000	HES7-12000	HES7-Ultrascale	HES7-BPx4 4xHES7-12000	HES7-BPx4 4xHES7-Ultrascale
FPGA Platform	**Xilinx Virtex-7**	**Xilinx Virtex-7**	**Xilinx UltraScale**	**Xilinx Virtex-7**	**Xilinx UltraScale**
Number of FPGAs	(Two) V7-2000 FHG1761 package Available also in dual V7-690	(Six) V7-2000T FLG1925 package	(Six) UltraScale-440 FLGA2892 package	(Twenty Four) V7-2000T FLG1925 package	(Twenty Four) UltraScale-440 FLGA2892 package
Single Board Capacity	Up to 24MG	Up to 72MG	Up to 158MG	288MG	633MG
Scalability with Backplane	Yes, up to 96MG	Yes, up to 288MG	Yes, up to 633MG	Multiple backplanes connected together	Multiple backplanes connected together
Global Clocks	• 5 clock modules • 60 GCK inputs • Total of 8 reference clock oscillators connected to main FPGAs	• 5 clock modules • 170 GCK inputs • 6 reference clock oscillators for main FPGAs GCK pins • 4 reference clock oscillators for main FPGAs GTX clocks	• 5 clock modules • 172 GCK inputs • 6 reference clock oscillators for main FPGAs GCK pins • 4 reference clock oscillators for main FPGAs GTX clocks	• 4x5 independent clock modules (1x5 per FPGA board) • 4 global clock modules for Backplane system (driven from Backplane board) • 24 reference clock oscillators for main FPGAs GCK pins • 16 reference clock oscillators for main FPGAs GTX clocks	• 4x5 independent clock modules (1x5 per FPGA board) • 4 global clock modules for Backplane system (driven from Backplane board) • 24 reference clock oscillators for main FPGAs GCK pins • 16 reference clock oscillators for main FPGAs GTX clocks
Connector type -External daughter boards	Molex	FMC Molex	FMC Molex	FMC Molex	FMC Molex
FPGA-FPGA interconnections	SE: 318 DIFF: 159	SE: 2036 DIFF: 977	SE: 2412 DIFF: 1200	SE: 9584 DIFF: 4628	SE: 11568 DIFF: 5760
Board-Backplane interconnections	SE: 720 DIFF: 360	SE: 720 DIFF: 360	SE: 960 DIFF: 480	SE: 1440 DIFF: 720	SE: 11568 DIFF: 960
Gbit FPGA-FPGA interconnections	16 GTX links	43 GTX links	115 GTH links	196 GTX links	548 GTH links
Gbit links FPGA-FMC interconnections	NA	12 GTX links	48 GTH links	48 GTX links	192 GTH links
Gbit FPGA-Backplane interconnections	44 GTX links	12 GTX links	44 GTH links	24 GTX links	88 GTH links
On board memories	• (Two) SO-DIMM DDR3 (each up to 8GB, with dedicated 200MHz reference clock) • microSD socket • SPI and NAND FLASH	• (Three) SO-DIMM DDR3 (each up to 8GB, with dedicated 200MHz reference clock) • microSD socket • SPI and NAND FLASH	• (Three)SO-DIMM DDR4 (each up to 8GB, with dedicated 200MHz reference clock) • microSD socket • SPI and NAND FLASH	• (Twelve) SO-DIMM DDR3 (each up to 8GB, with dedicated 200MHz reference clock) • (Four) microSD sockets • (Four) SPI and NAND FLASH	• (Twelve) SO-DIMM DDR4 (each up to 8GB, with dedicated 200MHz reference clock) • (Four) microSD sockets • (Four) SPI and NAND FLASH
Host Interface FPGA	Kintex-7 XC7K325T-FBG900	Virtex-7 XC7VX690T-FFG1926	Virtex-7 XC7VX690T-FFG1926	(Four) Virtex-7 XC7VX690T-FFG1926	(Four)Virtex-7 XC7VX690T-FFG1926
High speed interfaces to Host Interface FPGA	PCI-E x8 gen3 + USB3.0, SATA Host, Sata Device interfaces connected to FPGA1	• 1Gb ETH • 40Gb ETH (QSFP+) • USB 3.0 interface • (Two) PCI-E x8 gen3 • PCI-E x16 gen3 switchable to PCI-E x8 • (Two) Sata Host/Device interface	• 1Gb ETH • 40Gb ETH (QSFP+) • USB 3.0 interface • PCI-E x8 gen3 • PCI-E x16 gen3 switchable to PCI-E x8 • Sata Host/Device interface	• Four 1Gb ETH • Four 40Gb ETH (QSFP+) • Four USB 3.0 interface • (Eight) PCI-E x8 gen3 • (Four) PCI-E x16 gen3 switchable to PCI-E x8 • (Eight) Sata Host/Device interface	• Four 1Gb ETH • Four 40Gb ETH (QSFP+) • Four USB 3.0 interface • Four PCI-E x8 gen3 • Four PCI-E x16 gen3 switchable to PCI-E x8 • (Four) Sata Host/Device interface
Board Utility	HES7Proto (FPGA programming, board configuration)	HES7Proto (FPGA programming, board configuration)	HES7Proto (FPGA programming, board configuration)	HES7Proto (FPGA programming, board configuration)	HES7Proto (FPGA programming, board configuration)
Acceleration and Emulation Modes	Supported via HES-DVM	Supported via HES-DVM	Supported via HES-DVM	Supported via HES-DVM	Supported via HES-DVM
Multi User Support	Yes, Backplane configuration	Yes, Backplane configuration	Yes, Backplane configuration	Yes	Yes
Chassis	Yes Rack form factor	Yes Rack form factor	Yes Rack form factor	Yes Rack form factor	Yes Rack form factor