

DO-254/CTS™ | FPGA Level In-Target Testing

The FAA/EASA Guidance

DO-254/ED-80, "Design Assurance for Airborne Electronic Hardware" is currently recognized by the FAA and EASA as a means of compliance to the federal aviation regulations for the development of FPGAs, PLDs and ASICs used in commercial airborne systems.

The Challenges in Hardware Verification

Requirements-based physical testing is essential to satisfying both the objectives of DO-254 and interpretation of FAA Order 8110.105 and EASA CM-SWCEH-001. However, requirements-based testing using the target board is difficult and not feasible in most cases. Developers are faced with significant challenges such as:

- Limited FPGA I/O controllability and visibility
- Development of requirements-based test vectors
- Lack of robustness testing capabilities (voltage and CLK variations)
- Results capturing and documentation
- Lack of automation in the verification cycle

The Solution

DO-254/CTS™ is a fully customized device test system that augments target board testing to increase verification coverage by test and satisfy the verification objectives of DO-254/ED-80. The target design runs at-speed in the target device mounted on the custom daughter board. The simulation testbench is used as test vectors to enable requirements-based testing with 100% FPGA pin-level controllability and visibility necessary to implement normal range and abnormal range tests. The FPGA testing results are captured at-speed and displayed using a simulator waveform viewer for advanced analysis and documentation. The components of DO-254/CTS are:

- COTS Mother Board
- Custom Daughter Board
- Custom Software Package

Top Features

- At-speed testing in target device
- Reuse testbench as test vectors
- FPGA I/Os full visibility/controllability
- Early access to FPGA hardware board for device testing
- For use with Altera®, Lattice®, Microsemi® and Xilinx® devices
- Supports FPGAs with serial high speed I/Os (ARINC 818, PCIe, DDR3 and LVDS)
- Single environment to verify all FPGA level requirements
- Integration with 3rd Party RTL Simulator, Synthesis and P&R Tools

The Flow

Step 1: Functional simulation of the DUT using the RTL simulator. DO-254/CTS provides a plug-in that generates two sets of vectors (no changes to design & testbench):

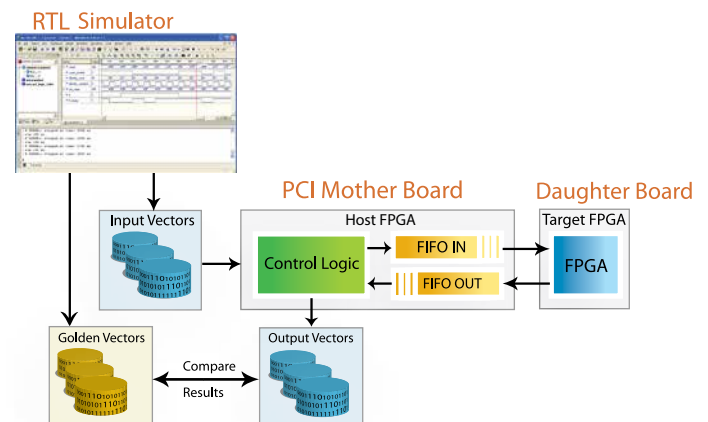
- **Input Vectors** - test vectors for hardware testing based on the testbench
- **Golden Vectors** - RTL simulation results which are used as basis for comparison

Step 2: Programming of DUT bit file to the FPGA daughter board.

Step 3: In-target testing at full speed with the mother board and daughter board using the Input Vectors as test vectors.

Step 4: Capturing of in-target testing results called Output Vectors.

Step 5: Comparison of Output Vectors with Golden Vectors using waveform viewer.



	Traditional Hardware Verification	DO-254 CTS Approach
Input Type	Real Data	RTL Test Vectors
Verification Type	At Speed	At Speed
Target Device	Yes	Yes
Test Data Generation	Manual Engineering Time Required	Automatic, No Additional Development Required
Test Environment Setup	Manual Connections of Wires and Cables	PCI/PCIe Based Hardware Boards
FPGA I/O Access	Limited Controllability	Complete Controllability & Visibility
Output Format	From Logic Analyzer, Oscilloscope	RTL Simulator Waveform Format
RTL and Hardware Results Comparison	Limited	Easy & Automated
FPGA Device Verification Time	Manual Process & Takes Years to Complete	Automated Process & Only Takes Weeks to Complete
Development Cost	Very High	Reduced Substantially

KEY Benefits

Augments Target Board Testing

To assess, at device level, that no unacceptable robustness defects remain, FPGA requirements-based testing should be defined to cover normal and abnormal input conditions. However, FPGA requirements-based testing is difficult using the target board. DO-254/CTS augments target board testing to facilitate requirements-based testing at the FPGA level.



DO-254/CTS Mother Board

Running at Required Operational Speed in excess of 250 MHz

Allows streaming of test vectors through the FPGA inputs at the required operational speed using real clocks in excess of 250 MHz. If the required simulation time is 500ms, then hardware testing completes within 500ms. Additional features to vary the frequency and voltage to +/-10% can also be used for robustness.

Automatic Generation of Test Vectors for Hardware Testing

Development of test vectors for hardware testing for an average Level A/B design normally takes 6-12 months manual engineering time. DO-254/CTS is equipped with a utility that converts the testbench within minutes into test vectors to be used for hardware testing.

Hardware Testing Results Visualization with Waveform Viewer

Allows capturing and visualization of results using the simulator's standard waveform viewer, providing storage for waveform files of up to 16TB and capturing of results immediately after simulation.

Single-Environment to Verify all FPGA Level Requirements

It consists of custom hardware with PCIe interface and software providing a single-environment to test all FPGA level requirements, specifically designed to avoid manual bypasses of cables and wires which are typically prone to errors and bugs.

Automated In-Hardware Testing

DO-254/CTS is a "push-button" automated in-hardware testing environment to test all FPGA level requirements. It is equipped with a utility to automatically compare RTL simulation results with hardware testing results. The utility displays either a PASS or FAIL message in which results can be further investigated using a standard waveform viewer.

Target Device Testing

The design must be tested in the target device per RTCA/DO-254 specification sections 1.1 and 6.3.1. DO-254/CTS consists of a custom daughter board that contains the specific family/package or part number of the FPGA/PLD device from vendors such as Altera, Lattice, Microsemi (Actel) and Xilinx.



DO-254/CTS Custom Daughter Board

Integration with 3rd Party RTL Simulator, Synthesis and P&R

DO-254/CTS can be used with any 3rd party RTL Simulator, Synthesis and P&R tools.

"EASA approved our verification process based on Aldec DO-254/CTS, accepted our test results, and the audit passed without any findings. This is the first time in Elbit's history that we have been able to bring more than 5 FPGA devices to the audit. Aldec helped us solve several of our verification challenges and delivered quick and professional responses for all our requests."

~ Moshe Porian,
Logic Design Verification Group Leader at
Elbit Systems Aerospace Division