

# FPGA Design and Simulation Made Easy



**Active-HDL™**

Active-HDL is an integrated FPGA Design and Simulation solution, with design entry, a high-performance mixed-language simulator and an easy-to-use, multi-vendor FPGA flow manager that controls simulation, synthesis and implementation for industry leading FPGA vendors (Altera®, Atmel®, Lattice®, Microsemi™ (Actel), Quicklogic® and Xilinx®) from one common environment. Active-HDL has interfaces to over 80 leading EDA tools, making it the most powerful platform.

## Top Features

- Graphical Design Entry
- High Performance Mixed-Language RTL Simulator
- IEEE VHDL, Verilog®, SystemVerilog (Design), SystemC
- Advanced Debugging & Code Coverage
- IP Encryption based on IEEE Standards
- Assertion-Based Verification (ABV)
- DSP Co-simulation with MATLAB®/Simulink®
- PCB Design Interface
- HTML and PDF Design Documentation
- Windows® 7/Vista/XP/2003 32/64 bit support

## Graphical Design Entry

Draw any finite state machine diagram and let Active-HDL generate your synthesizable RTL code. Connect all design modules at the top-level and automatically generate output structural HDL using the built-in block diagram editor. If needed, convert HDL to graphics with Code2Graphics™ utility. Active-HDL can also import, re-target, enhance, simulate and debug your legacy designs.



## High Performance, Mixed-Language Simulation

Active-HDL includes a high performance, common-kernel, mixed-language simulator supporting batch mode simulation, VCD, a performance profiler, memory viewer, encrypted IP and FPGA vendor libraries. Drive your system-level simulation model using complex testbenches or create quick and flexible stimulator farms to rapidly test design modules and system-level designs.

## Debugging and Code Coverage

Active-HDL includes state-of-the-art debugging with an Accelerated Waveform, with cross-probing to HDL source code, breakpoint management, testbench and stimulus generation. A powerful HDL code coverage analyzer provides 100% test coverage of all statements, lines, signals, toggle, branch, path and logical expressions in the design.

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STANDARDS



SILICON



INTERFACES



FEATURES

PRODUCT CONFIGURATIONS

	DM	Designer Edition	PE	EE
<b>Design Entry and Documentation</b>				
HDL, Text, Block Diagram and State Machine Editor	.	.	.	.
Language Assistant with Templates and Auto-Complete	.	.	.	.
Macro, Tcl/Tk, Perl script Support	.	.	.	.
Code2Graphics™ Converter	.	.	.	.
Legacy Schematic Design Import and Symbol Import/Export	.	.	.	.
Export to PDF/HTML/Bitmap Graphics	.	.	.	.
Advanced Export to PDF (Vector Graphics)	Option	.	.	.
<b>Project Management</b>				
Design Flow Manager for All FPGA Vendors	.	.	.	.
Revision Control Interface	.	.	.	.
PCB Interface	.	.	.	.
<b>Code Generation Tools</b>				
IP Core Component Generator	.	.	.	.
Testbench Generation from Waveforms	.	.	.	.
Testbench Generation from State Diagram	.	.	.	.
<b>Supported Standards</b>				
VHDL IEEE 1076 (1987, 1993, 2002 and 2008)	.	.	.	.
Verilog® HDL IEEE 1364 (1995, 2001 and 2005)	.	.	.	.
SystemVerilog IEEE 1800™-2005 (Design)	.	.	.	.
EDIF 2.0.0	.	.	.	.
SystemC™ 2.2 IEEE 1666™/OSCI 2.2/TLM 2.0	.	.	Option	.
<b>Simulation/Verification</b>				
Simulation Performance (Baseline 2X Faster than FPGA Vendor Supplied Simulator)		Baseline	3X Baseline	Up To 6X Baseline
Single or Mixed Language Design Support	Mixed Only	Mixed Only	.	.
Simulation Model Protection/Library Encryption	.	.	.	.
VHDL/Verilog IEEE Compatible Encryption	.	.	.	.
Value Change Dump (VCD and Extended VCD) Support	.	.	.	.
Verilog Programming Language Interface (PLI/VPI)	.	.	.	.
VHDL Programming Language Interface (VHPI)	.	.	.	.
Batch Mode Simulation/Regression (VSimSA)	.	.	.	.
Pre-compiled FPGA Vendor Libraries	.	.	.	.
Xilinx SecureIP Support	.	.	Option	.
Altera® Language-Neutral Libraries	.	.	Option	.
Profiler (Performance Metrics)	.	.	Option	.
Verilog HDL Simulation Optimization	.	.	.	.
VHDL Simulation Optimization	.	.	.	.
SFM (Server Farm Manager)	.	.	Option	Option
<b>HDL Debug and Analysis</b>				
Interactive Code Execution Tracing	.	.	.	.
Advanced Breakpoint Management	.	.	.	.
Memory Viewer	.	.	.	.
Waveform Viewer	.	Viewer Only	.	.
Waveform Stimulator	.	.	.	.
Waveform Comparison and Editing	.	.	.	.
Post-Simulation Debug	.	.	.	.
C++ Debugger	.	.	.	.
Signal Agent (VHDL and Mixed Only)	.	.	.	.
X-Trace	.	.	Option	.
Advanced Dataflow	.	.	Option	.
Integration with Riviera-PRO and ALINT	Option	.	Option	.
Assertions Debugging	.	.	Option	Option
Synopsys® SmartModels, SWIFT interface and LMTV	.	.	Option	.
<b>Assertions and Coverage Tools</b>				
UCIS-compatible Aldec Coverage Database	.	.	Option	.
Code, Statement, Branch, Expression, Condition and Toggle Coverage	.	.	Option	.
PSL IEEE 1850, SystemVerilog IEEE 1800™, OpenVera Assertions	.	.	Option	Option
Path Coverage (VHDL Only)	.	.	.	.
<b>Design Rule Checking</b>				
ALINT™ with Aldec Basic Rule Library	.	.	Option	.
DO-254 VHDL or Verilog Rule Library	.	.	Option	Option
STARC® VHDL or Verilog Rule Library	.	.	Option	Option
RMM Verilog and VHDL Rule Library	.	.	Option	Option
<b>Co-Simulation</b>				
Simulink® Co-Simulation	.	.	.	.
MATLAB® Co-Simulation	.	.	Option	.
<b>Supported Platforms</b>				
Windows® 7/Vista/XP/2003 32/64 bit	.	.	.	.

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