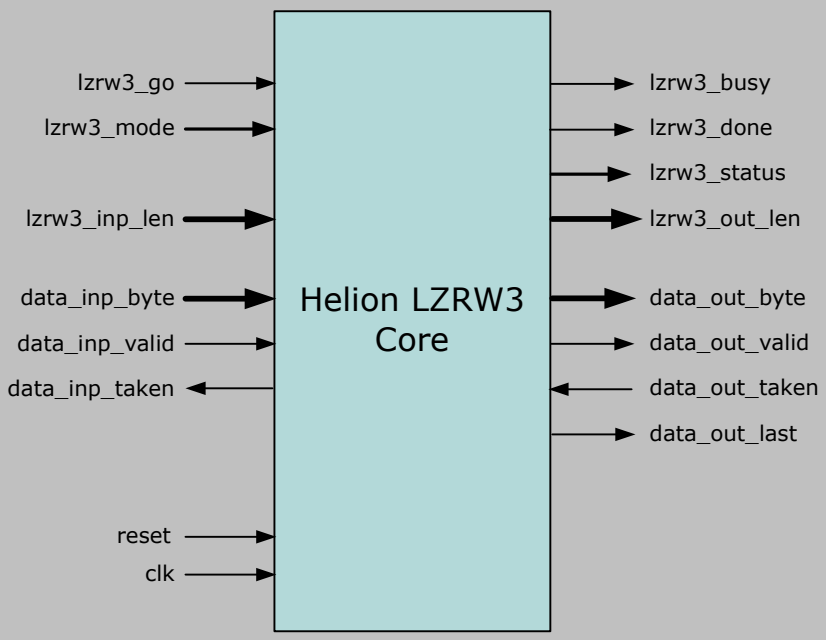
Helion Technology

FULL DATASHEET – LZRW3 Data Compression Core for FPGA



Features

- Implements the LZRW3 lossless data compression algorithm
- Available as Compress only, Expand only, or Compressor/Expander core
- Supports data block sizes from 2K to 32K bytes with data growth protection
- Completely self-contained; does not require off-chip memory
- High performance; capable of data throughputs in excess of 1 Gbps
- Highly optimised for use in each FPGA technology
- Ideal for improving system performance in data comms and storage applications

Deliverables

- Target specific netlist or fully synthesisable RTL VHDL/Verilog
- VHDL/Verilog simulation model and testbench
- Comprehensive User documentation

Overview

The Lempel-Ziv (LZ) compression methods are among the most popular algorithms for lossless data compression. LZ methods use a table based compression model where table entries are substituted for repeated strings of data.

LZRW3 is a well known LZ-type algorithm developed by Ross Williams in the 1990s which offers a useful combination of high throughput and good compression performance. It also has the advantage of being very efficient to build in hardware, unlike the majority of compression algorithms which tend to favour software implementations.

The Helion LZRW3 core implements the LZRW3 data compression algorithm in FPGA without the need for external memory storage. It is capable of handling data throughputs in excess of 1 Gigabit/sec, and is ideal for use for improving system performance and efficiency in data communications, networking and data storage applications.

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General Description

The Helion LZRW3 core operates on one input block at a time. An LZRW3 operation is started whenever the "go" input to the core is asserted and the core is not busy. The data input length and mode inputs need to be valid during the go cycle, after which processing starts; the core busy flag is asserted whilst compression or decompression is in progress. Whilst the core is busy, data can be passed into the core for processing. The data input and output interfaces are byte-wide, and use associated data flow control signals to transfer data to/from the core. Input data is pushed into the core by the user application, and output data is pushed out from the core to the user application.

Once a whole data block has been processed, a single cycle pulse is output on "done" to indicate when the core is finished as well as to indicate the output length in bytes and status outputs are valid. The status output shows whether the compression attempt was successful or not. Further block processing can then be started.

The Helion LZRW3 core processes data at a *peak rate* of 1 byte per clock on the fastest (uncompressed) interface; obviously the slower interface (compressed) will be at a lower rate than this. The actual rate depends on exactly what is happening in the internal pipeline of the core at any one time, which by the very nature of data compression/ expansion is data dependent. As a generalisation however, the data rate is typically 70-90% of this maximum for both compression and expansion.

Logic Utilisation and Performance

Helion has a long history in high-end FPGA design, and we therefore take great care when implementing our IP cores. As a result they have been designed from the ground up to be highly optimal for each individual FPGA technology - they are not simply based on a synthesised generic RTL ASIC design. The Helion LZRW3 core makes use of the architectural features available in each FPGA technology to achieve the highest performance combined with the most efficient logic resource utilisation.

The latest logic area, performance figures, and datasheets for the Helion LZRW3 core in a range of different technologies are available at http://www.heliontech.com/compression.htm. Please feel free to contact Helion for further details on both the compression and throughput performance of the core.

About Helion

Helion is a long established British company based in Cambridge, England, offering a range of product-proven Data Security silicon IP cores backed up by our highly experienced and professional design service capabilities. Although we specialise in providing the highest performance data encryption and authentication IP, our interest does not stop there. Unlike broadline IP vendors who try to supply a very diverse range of solutions, being specialists we can offer much more than just the IP core itself.

For instance, we are pleased to be able to supply up-front expert advice on any security applications which might take advantage of our technology. Many of our customers are adding data security into their existing systems for the first time, and are looking for a little assistance with how best to achieve this. We are pleased to help with suitable advice and support where necessary, and pride ourselves in our highly personal approach.

The quality of our IP is however the main reason our customers keep coming back for more. We passionately believe that if you are buying IP, it should have been designed with the ultimate in care, crafted to achieve the ultimate performance in each target technology, and thoroughly tested to ensure compliance with any associated standards. All this comes as standard with IP from Helion.

More Information

For more detailed information on this or any of our other products and services, please contact Helion and we will be pleased to discuss how we can assist with your individual requirements.

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