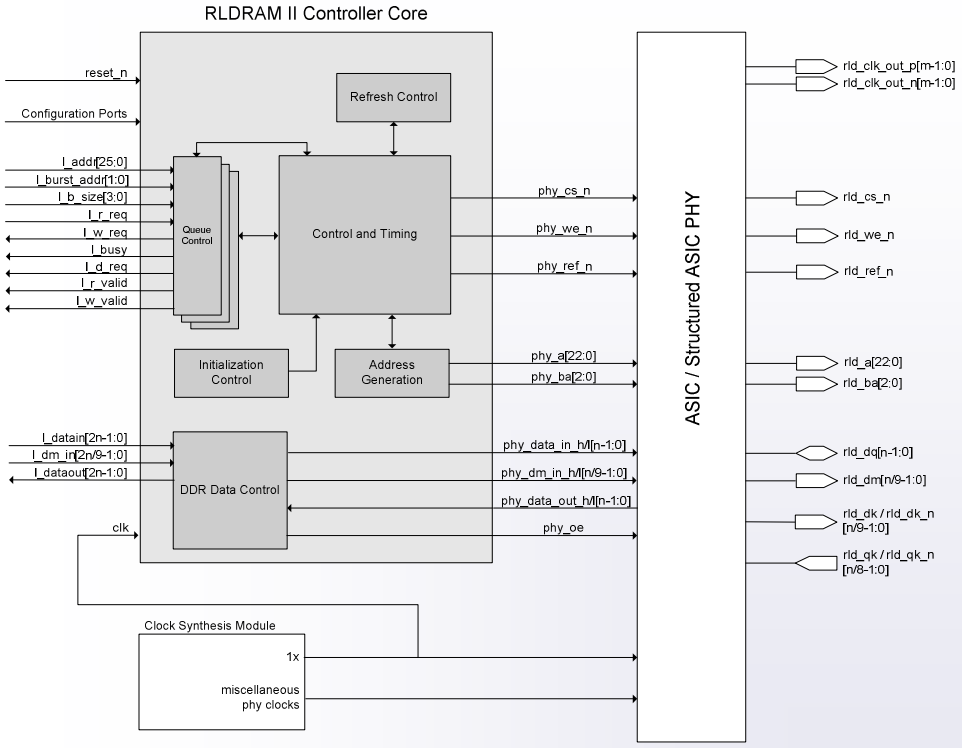
RLDRAM II Controller Core

Product Highlights

- Achieves high clock rates with minimal routing constraints
- Minimal latency achieved via parameterized pipelining
- Supports full rate and half-rate clock operation
- Full run-time configurable timing parameters and memory settings
- Full set of Add-On Cores available
- Delivered fully integrated and verified with target DDR PHY
- Minimal ASIC gate count
- Broad range of ASIC and FPGA platforms supported
- Source code available
- Customization and Integration services available

Block Diagram



Product Overview

Northwest Logic's Reduced Latency DRAM (RLDRAM) II Controller Core is designed for use in applications requiring high memory throughput, high clock rates and full programmability.

The core has been optimized to take advantage of the fast random cycle and fast access times available with RLDRAM II. The core also supports both common and separate data buses and multiplexed and non-multiplexed addressing.

The core accepts commands using a simple local interface and translates them to the command sequences required by RLDRAM II devices. The core also performs all initialization and refresh functions.

The core is provided with run-time programmable inputs for all memory timing parameters and configuration settings. This ensures compatibility with all RLDRAM II configurations. Add-On Cores such as a Multi-Port Front-End and Reorder Core can be optionally delivered with the core. The core is deiiv-ered fully integrated and verified with the target DDR PHY. Northwest Logic supports a broad range of third party and its own soft DDR PHY. Contact Northwest Logic for more information.

Northwest Logic also provides IP Core customization services. Contact Northwest Logic for a quote.

Product Deliverables:

- Core (Netlist or Source Code)
- Testbench (Source Code) with support for Aldec
- Complete Documentation
- Expert Technical Support & Maintenance Updates