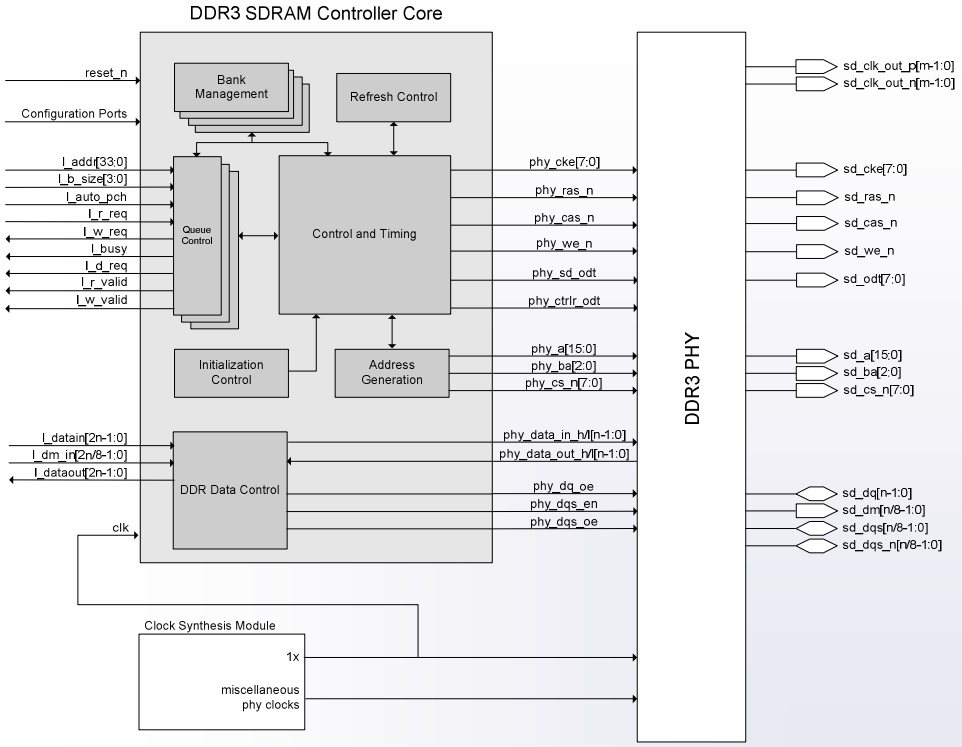
DDR3 SDRAM Controller Core

Product Highlights

- Maximizes bus efficiency via Look-Ahead command processing, Bank Management, Auto-Precharge and Additive Latency support
- Minimal latency achieved via parameterized pipelining
- Achieves high clock rates with minimal routing constraints
- Supports full rate and half-rate clock operation
- Full run-time configurable timing parameters and memory settings
- Supports ODT, dynamic ODT, 2T timing and write leveling calibration
- Full set of Add-On Cores available
- Delivered fully integrated and verified with target DDR PHY
- Minimal ASIC gate count
- Broad range of ASIC and FPGA platforms supported
- Source code available
- Customization and Integration services available

Block Diagram



Product Overview

Northwest Logic's Double Data Rate 3 (DDR3) SDRAM Controller Core is designed for use in applications requiring high memory throughput, high clock rates and full programmability.

The core accepts commands using a simple local interface and translates them to the command sequences required by DDR3 SDRAM devices. The core also performs all initialization, refresh and power-down functions.

The core uses bank management modules to monitor the status of each SDRAM bank. Banks are only opened or closed when necessary, minimizing access delays. Up to 32 banks can be managed at one time.

The core queues up multiple commands in the command queue. This enables optimal bandwidth utilization for both short transfers to highly random address locations as well as longer transfers to contiguous address space. The command queue is also used to opportunistically perform look-ahead activates, precharges and auto-precharges further improving overall throughput.

The core is provided with run-time programmable inputs for all memory timing parameters and configuration settings. This ensures compatibility with all DDR3 SDRAM configurations. The core also supports of ODT, dynamic ODT, 2T timing and write leveling calibration.

Add-On Cores such as a Multi-Port Front-End and Reorder Core can be optionally delivered with the core. The core is delivered fully integrated and verified with the target DDR PHY. Northwest Logic supports a broad range of third party and its own soft DDR PHY. Contact Northwest Logic for more information.

Northwest Logic also provides IP Core customization services. Contact Northwest Logic for a quote.

Product Deliverables:

- Core (Netlist or Source Code)
- Testbench (Source Code) with support for Aldec
- Complete Documentation
- Expert Technical Support & Maintenance Updates