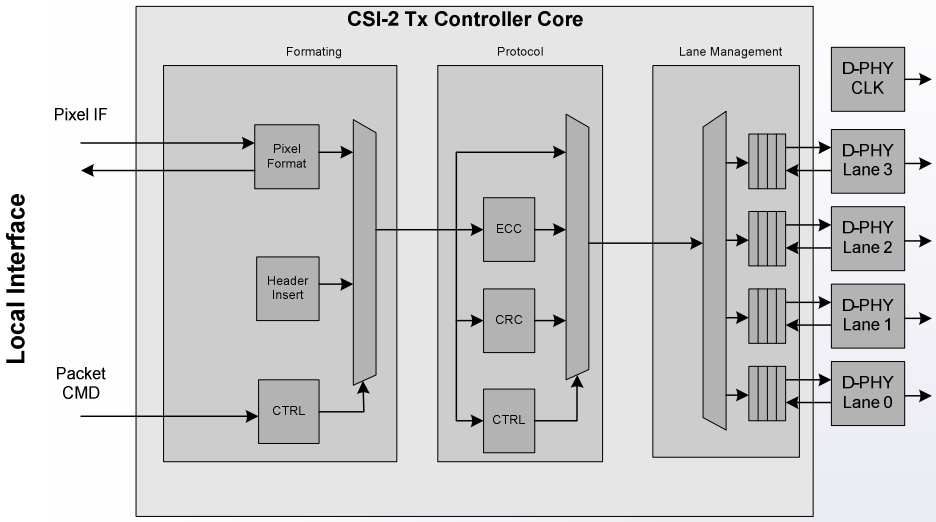
CSI-2 Controller Core

Product Highlights

- High-performance, easy-to-use core
- Fully CSI-2 Specification compliant
- Transmit and Receive versions
- 1-4 data lane support
- Support for all data types
- Supports high speed (1.5+ Gbit/s) and low power operation
- Delivered fully integrated and verified with target MIPI PHY
- Easy to use pixel-based user interface (single, double, quad)
- Provided with a MIPI CSI-2 Testbench
- Minimal ASIC gate count
- Source code available
- Customization and Integration services available
- Complete FPGA-based demonstration system available

Block Diagram (Transmitter Version)



Product Overview

The CSI-2 Controller Core is part of Northwest Logic's MIPI Solution. This solution is designed to achieve maximum MIPI throughput while being easy to use.

The core implements all three layers defined by the CSI-2 Specification: Pixel to Byte Packing, Low Level Protocol, and Lane Management and is fully compliant with the CSI-2 specification. Separate Transmit (Tx) and Receive (Rx) versions of the core are provided.

The core supports 1 to 4 data lanes at rates 1.5+ Gbit/s and all data types. The core's Local Interface is an easy to use pixel based interface (single, double, quad pixel wide).

The core uses the byte lane clock minimizing power consumption and ensuring the core can be used in older process technologies.

The core is delivered fully integrated and verified with the user's target MIPI PHY. Contact Northwest Logic for a complete list of supported PHYs.

The core is also provided with the MIPI CSI-2 Testbench which provides a MIPI CSI-2 Bus Functional Model.

Northwest Logic also offers a CSI-2 Demonstration System which includes an FPGA Board, MIPI Interface Card and MIPI Camera. Contact Northwest Logic for more information.

Northwest Logic also provides a complete set of quick-turn design services including IP Customization and Logic, Board, Software Development services. Contact Northwest Logic for a quote.

Product Deliverables:

- Core (Netlist or Source Code)
- Testbench (Source Code) with support for Aldec
- Complete Documentation
- Expert Technical Support & Maintenance Updates