



Getting Started with UVM/OVM using Riviera-PRO

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Abstract

This document briefly describes how to use UVM/OVM with Riviera-PRO. Each of these libraries provides robust framework for coverage-driven verification (CDV) – combines automatic test generation, self-checking testbenches, and coverage metrics to significantly reduce the design verification time.



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Introduction

This document describes how to use UVM and OVM SystemVerilog verification libraries with Riviera-PRO. It has been tested on Riviera-PRO 2010.10 and is fully compatible with the latest version of the product. If you have any questions about compatibility or this document in general, please do not hesitate to contact Aldec support at <http://support.aldec.com>.

Riviera-PRO is shipped with both UVM and OVM sample designs – they are available under the following folder (\$aldec indicates the installation path):

- \$aldec/examples/systemverilog/uvm-1.0.ea
- \$aldec/examples/systemverilog/ovm-2.1.1

Compiling UVM/OVM Based Environment

There are two choices to compile a UVM/OVM based verification environment:

1. Import the package into your design using the **import** uvm_pkg:* statement.
2. Include the UVM header file in all design files that use the library: ``include "uvm.svh"`. All design files must be compiled with a single compilation command.

Using Package Import (Riviera-PRO 2010.10 or later)

When using import (uvm_pkg, ovm_pkg) based compilation:

1. Specify the appropriate file (uvm_pkg.sv, ovm_pkg.sv) in the compiler command line. Location:
 - \$aldec/vlib/uvm-1.0.ea/src
 - \$aldec/vlib/ovm-2.1.1/src
2. Define the ALDEC macro (+define+ALDEC).

Example – compilation command for package based approach (test.sv is the user design file):
`alog +incdir+"$aldec/vlib/uvm-1.0.ea/src" +define+ALDEC \
"$aldec/vlib/uvm-1.0.ea/src/uvm_pkg.sv" test.sv`

Using File Include (Riviera-PRO 2010.06)

When using this approach:

1. Point to the include directory for the UVM files – this is the src/ directory from UVM distribution – in Riviera-PRO this directory is located in:
 - \$aldec/vlib/uvm-1.0.ea/src. (+incdir+"\$aldec/vlib/uvm-1.0.ea/src")
 - \$aldec/vlib/ovm-2.1.1/src. (+incdir+"\$aldec/vlib/ovm-2.1.1/src")
2. Define the ALDEC macro (+define+ALDEC).

Example – compilation command for include based approach (test.sv is the user design file):
`alog +incdir+"$aldec/vlib/uvm-1.0.ea/src" +define+ALDEC test.sv`



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Simulating UVM/OVM Based Environment

After design source files are compiled successfully, you can initialize the simulation with “asim” command. The simulation can then be started with the “run” command.

Please note that the messages prefixed with "ALDEC DEBUG" string may be printed during the simulation. To suppress those messages, please edit the file “aldec_ovm_include.vf” under “aldec/vlib/uvm-1.0.ea/src” or “aldec/vlib/ovm-2.1.1/src” and set the value for “ALDEC_DEBUG” to “0”.

Note – these messages are related to modifications (workarounds) that have been made to the original UVM and OVM sources. The modifications do not affect the operation of the libraries and are transparent to the end user.

About Aldec, Inc.

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